

Compal Confidential

Hasswell M/B Schematics Document

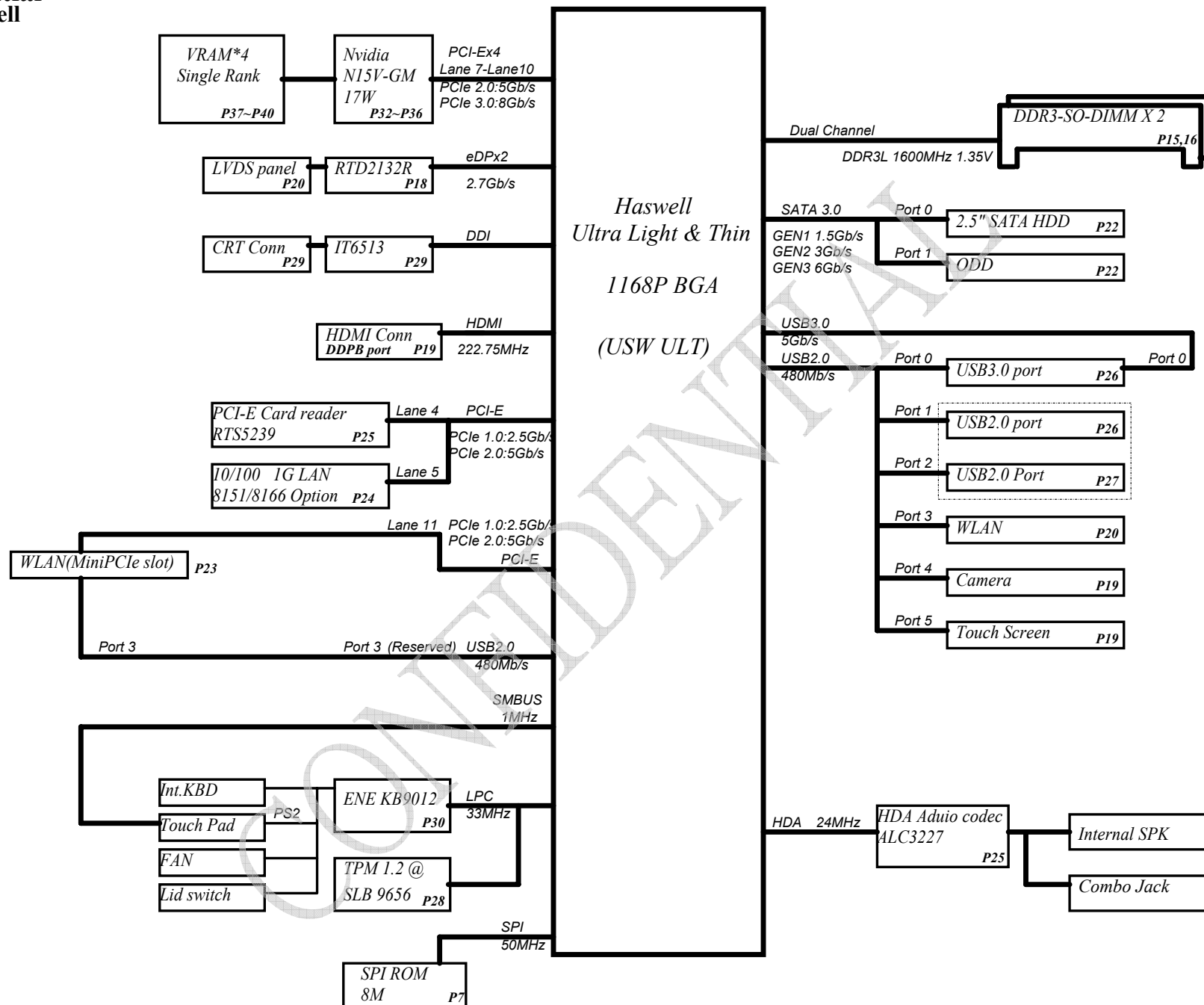
Intel ULV Processor with DDRIII L

Date : 2014/02/08

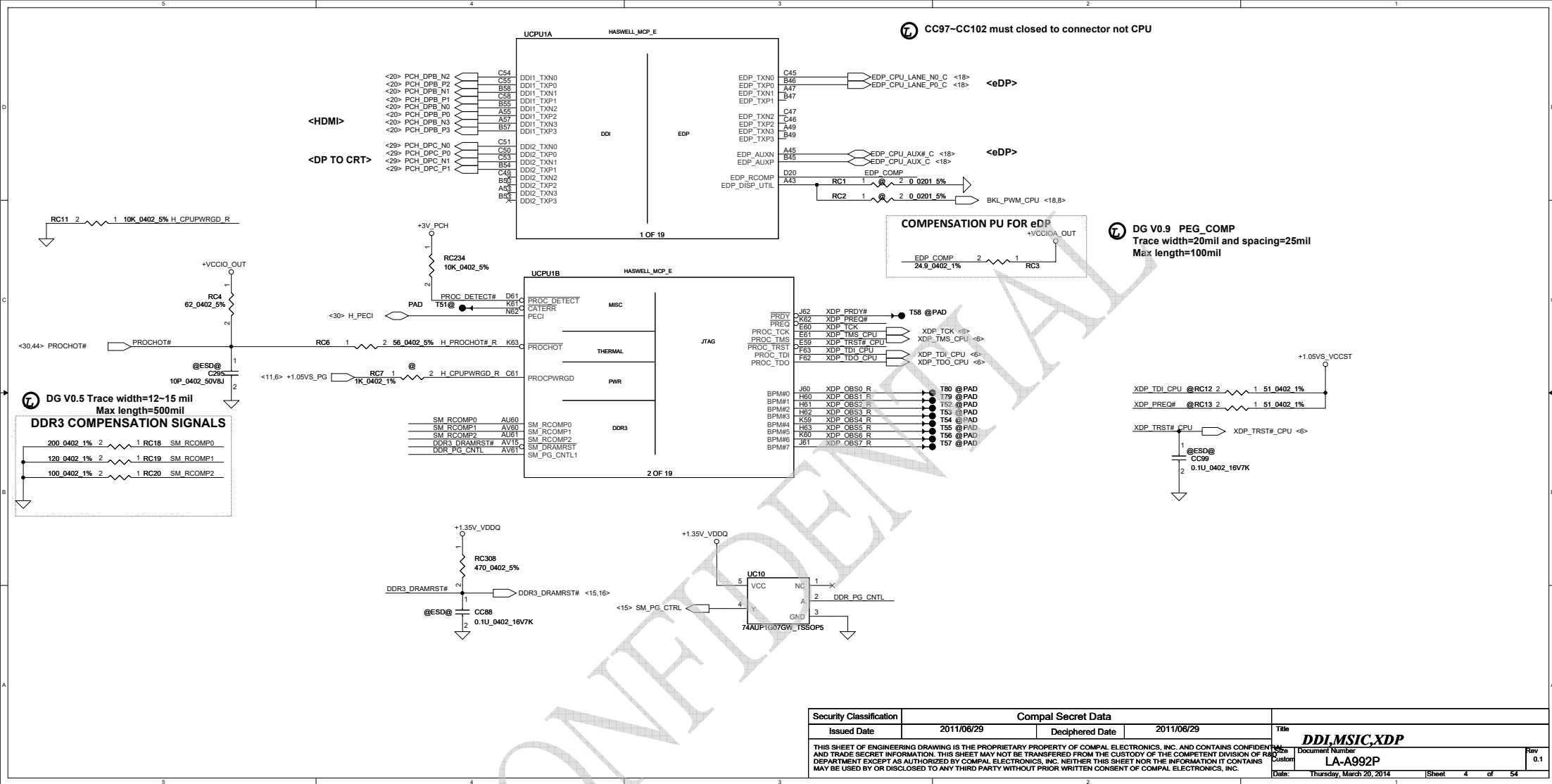
Version 1.0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	Cover Page
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Date: Thursday, March 20, 2014		Sheet 1 of 54			

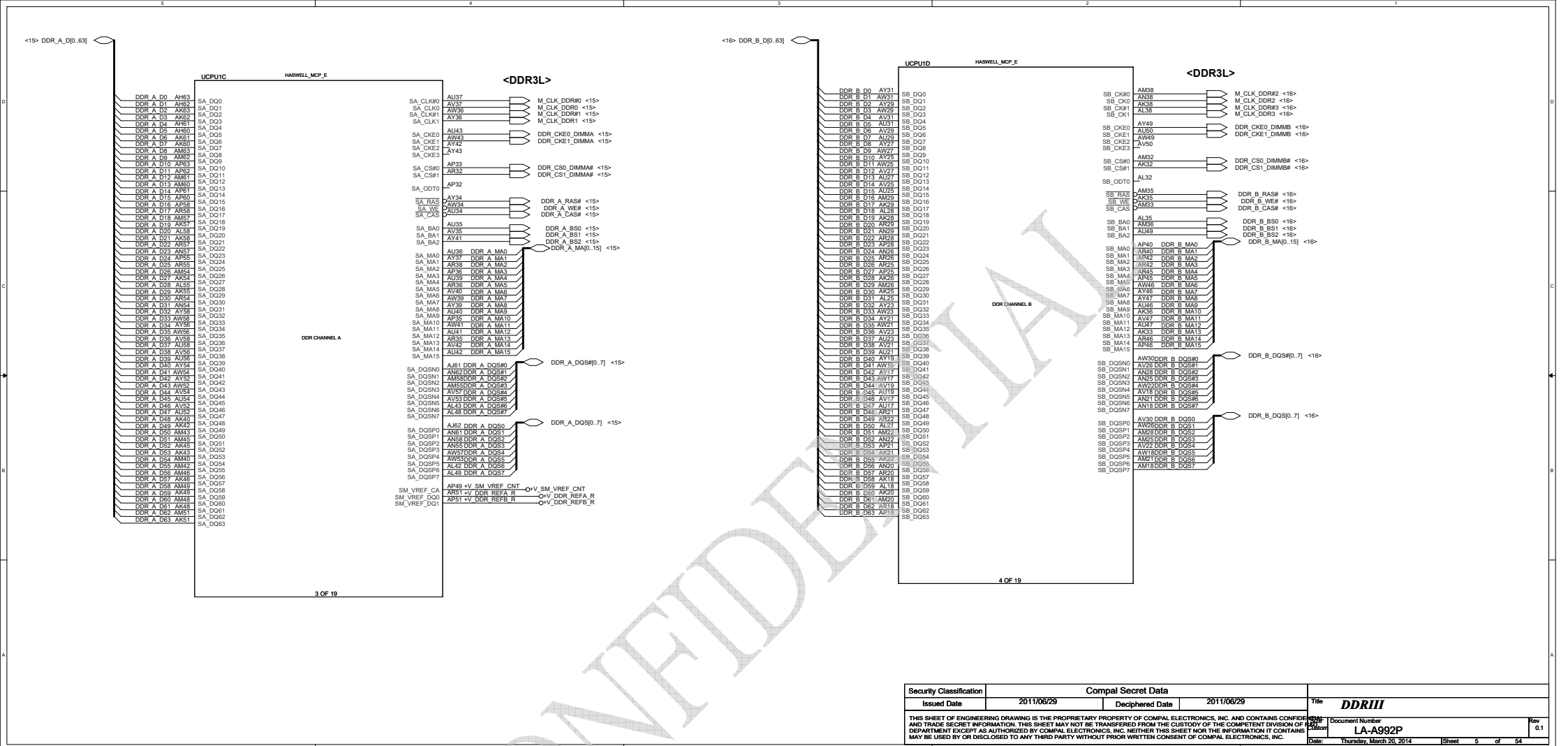
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LA-A992PR10

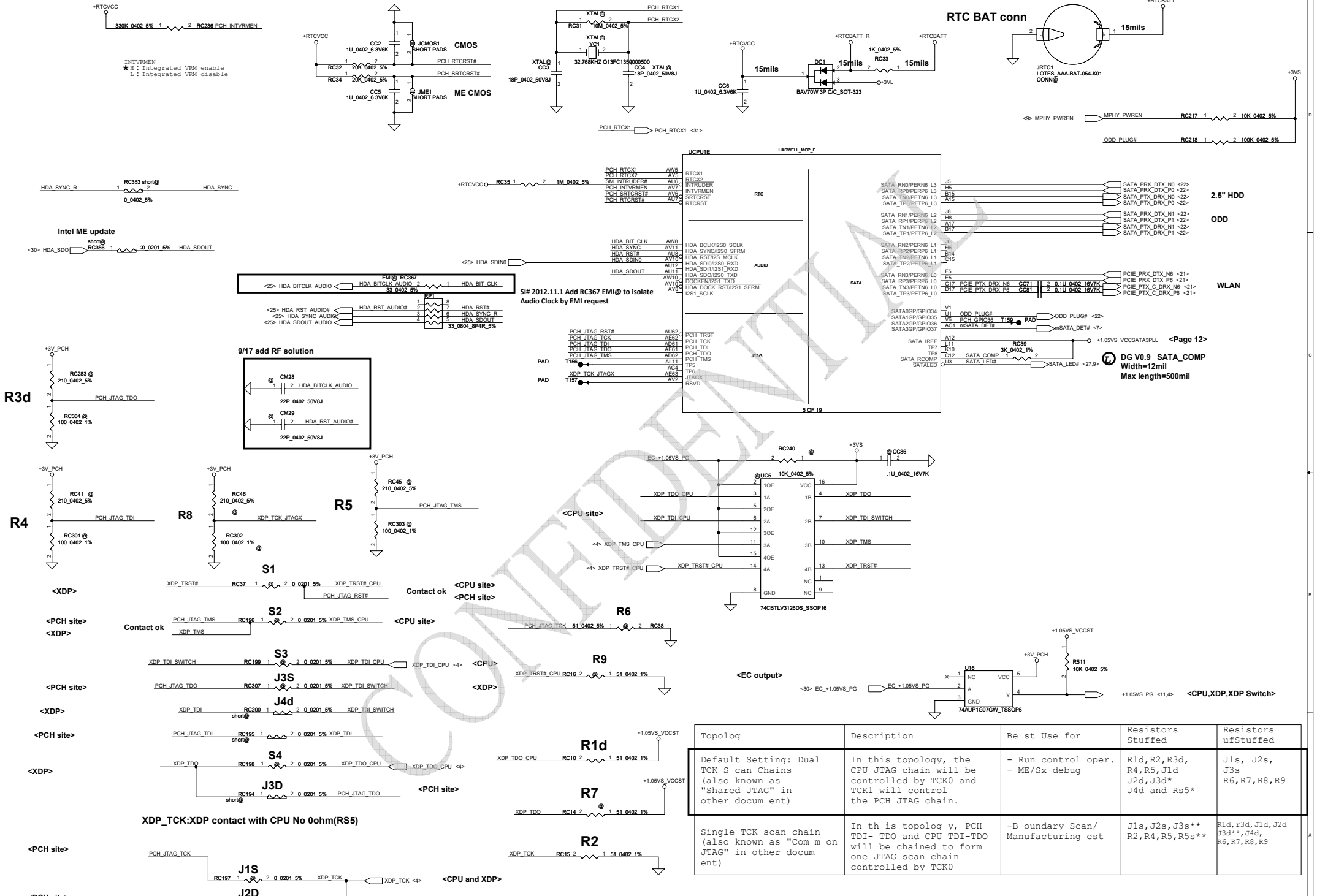


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	Block Diagrams
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				Date: Thursday, March 20, 2014	Sheet 2 of 54

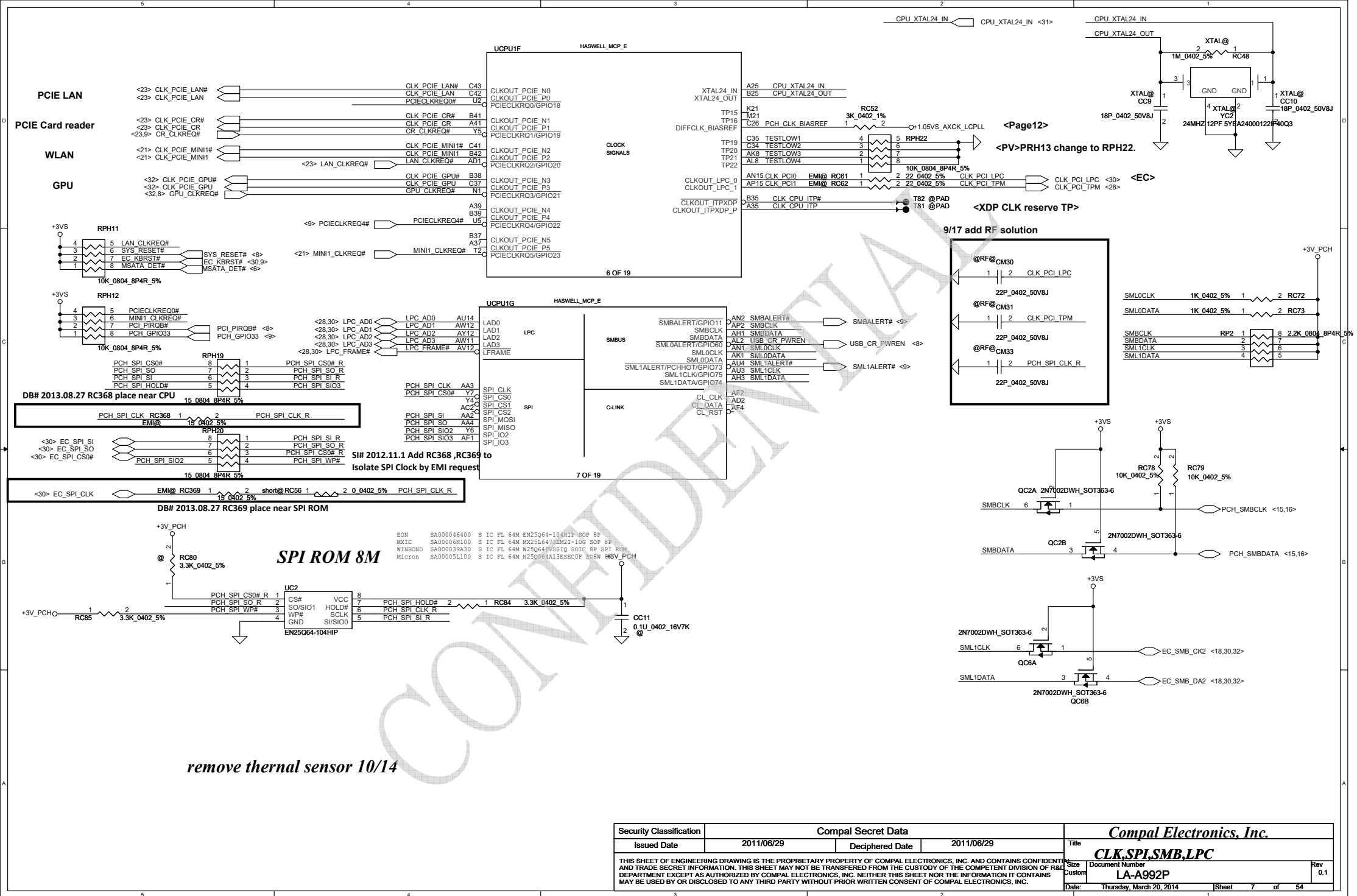


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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	DDRIII
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				Document Number	LA-A992P
				Date:	Thursday, March 20, 2014
				Sheet	5 of 54
				Rev	0.1





Topolog	Description	Be st Use for	Resistors Stuffed	Resistors uStuffed
Default Setting: Dual TCK S can Chains (also known as "Shared JTAG" in other docum ent)	In this topology, the CPU JTAG chain will be controlled by TCK0 and TCK1 will control the PCH JTAG chain.	- Run control oper. - ME/Sx debug	R1d,R2,R3d, R4,R5,J1d J2d,J3d* J4d and Rs5*	J1s, J2s, J3s R6,R7,R8,R9
Single TCK scan chain (also known as "Com m on JTAG" in other docum ent)	In th is topology, PCH TDI- TDO and CPU TDI-TDO will be chained to form one JTAG scan chain controlled by TCK0	-B oundary Scan/ Manufacturing est	J1s,J2s,J3s** R2,R4,R5,R5s**	R1d,r3d,J1d,J2d J3d** ,J4d, R6,R7,R8,R9



Non Deep S3 RC91-->SMT
Deep S3 RC93-->SMT

Deep S3

PANEL_BKEN_CPU PD 100K on Page20

PD on KBC page

DSWODVREN - On Die DSW VR Enable

* H : Enable
L : Disable

DSWODVREN RC254 2 1 330K 0402 5%

DSWODVREN RC255 2 1 330K 0402 5%

Deep S3:DSW power choose on page12

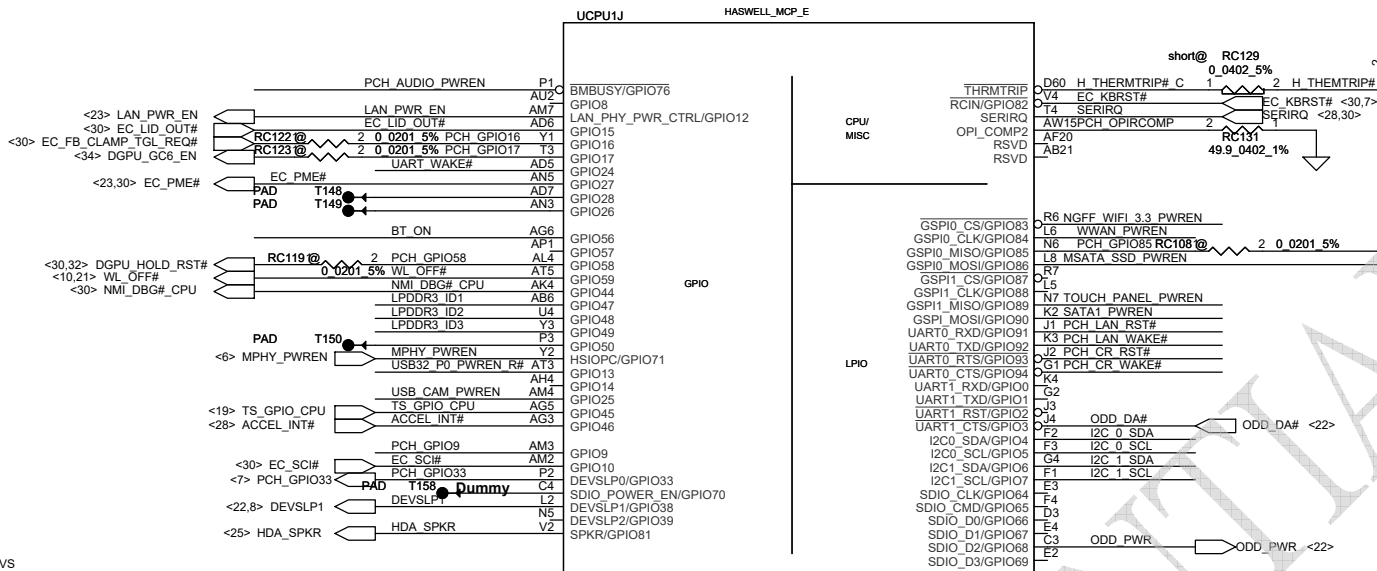
<S>Displayport Port C Enable pin RC102 pull high +3VS

<DP TO CRT HPD>

<HDMI>
<DP TO CRT HPD>
<eDP HPD>

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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Size	Custom
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				LA-A992P	0.1
Date				Thursday, March 20, 2014	Sheet 8 of 54

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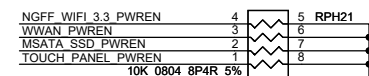


DG V0.9 PCH_OPIRCOMP
Width=12mil,spacing=12mil
Max length=500mil

Boot BIOS Strap

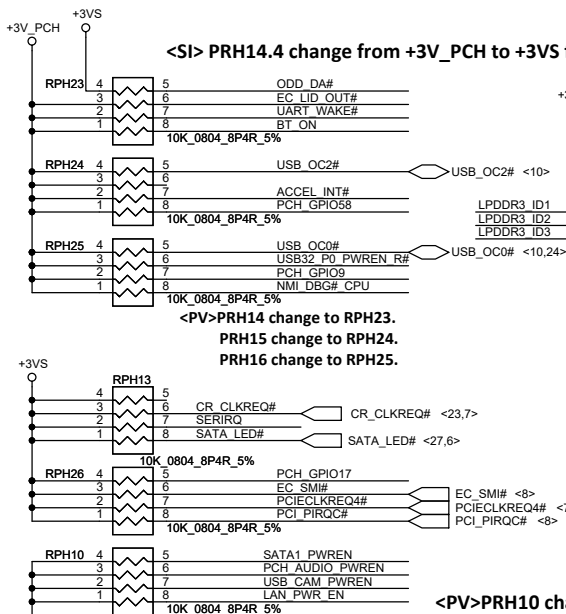
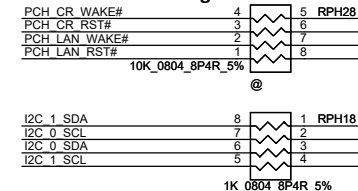
PCH_GPIO86	Boot BIOS Location
0	SPI

9/12 reserve DGPU_PWR_EN on GPIO85



<PV>PRH12 change to RPH21.

<PV>PRH19 change to RPH28.



<PV>PRH10 change to RPH10.
PRH17 change to RPH26.

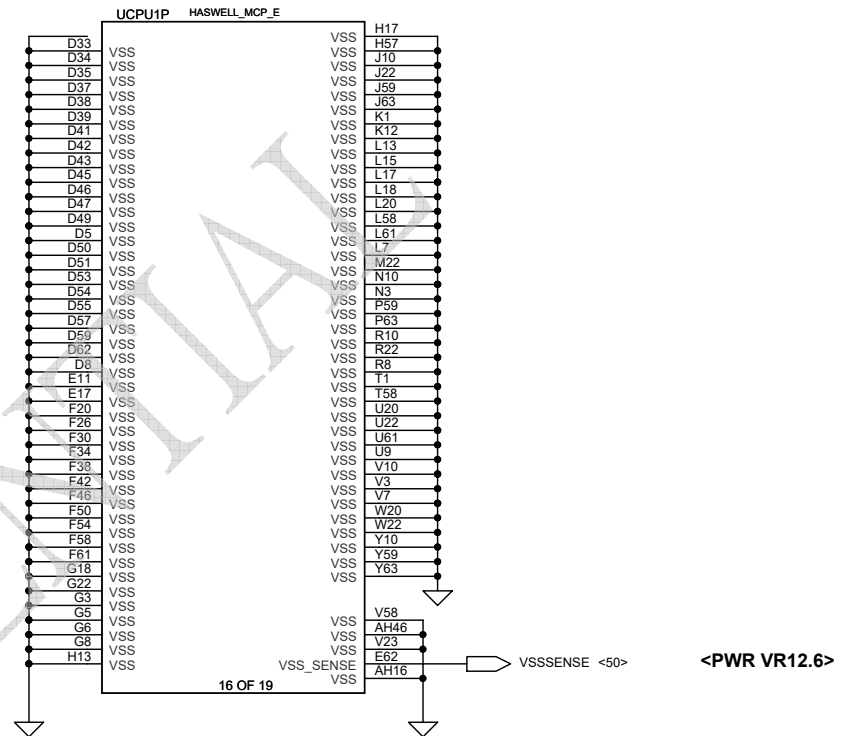
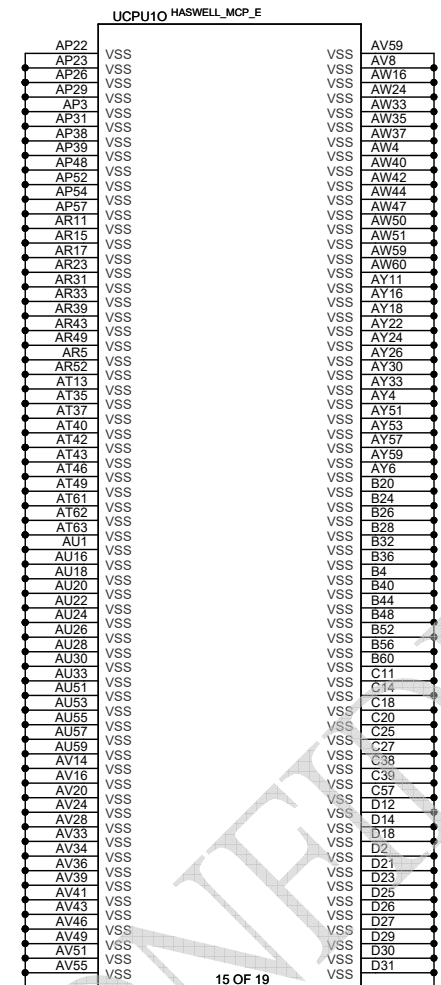
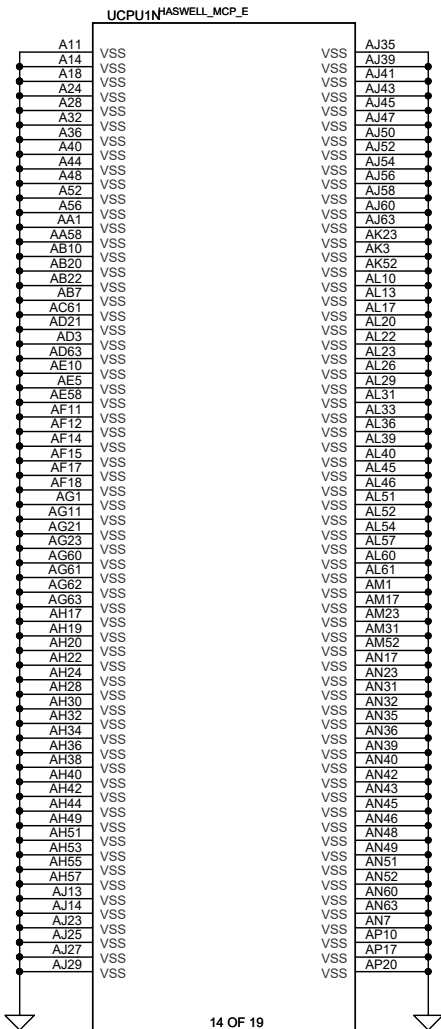
DSW power choose on page12

PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

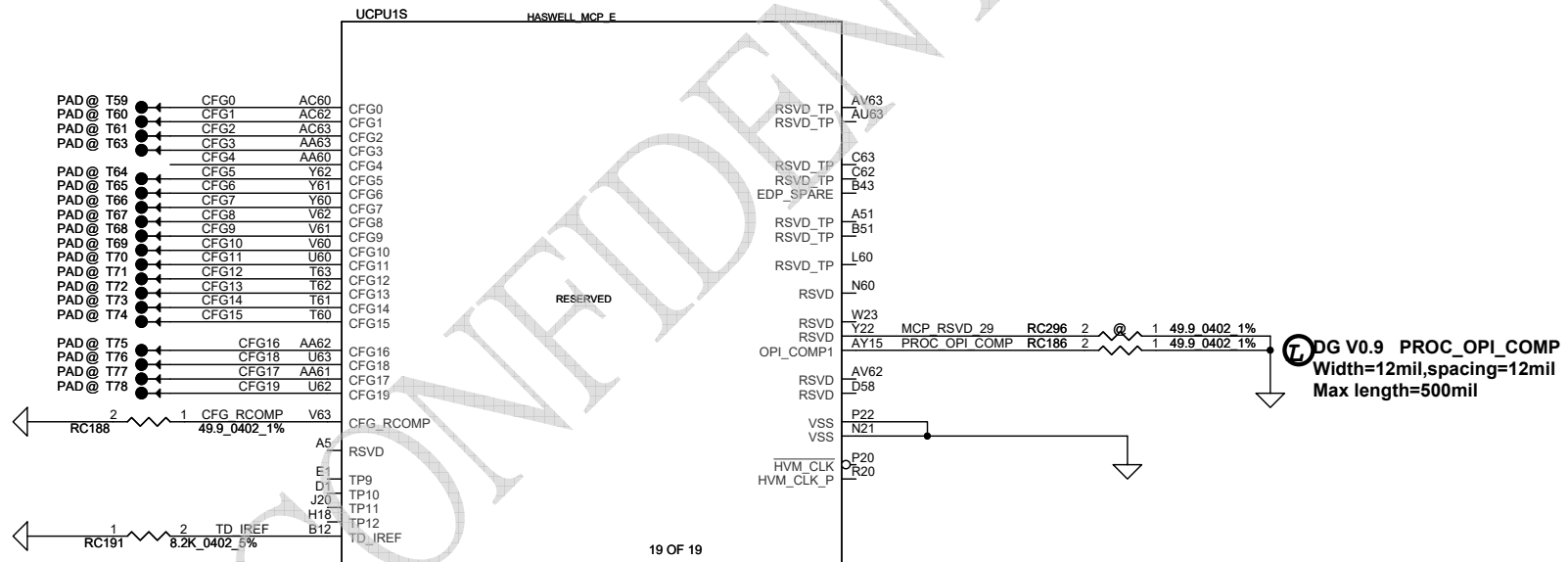
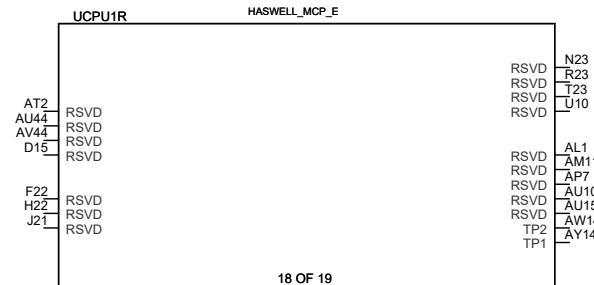
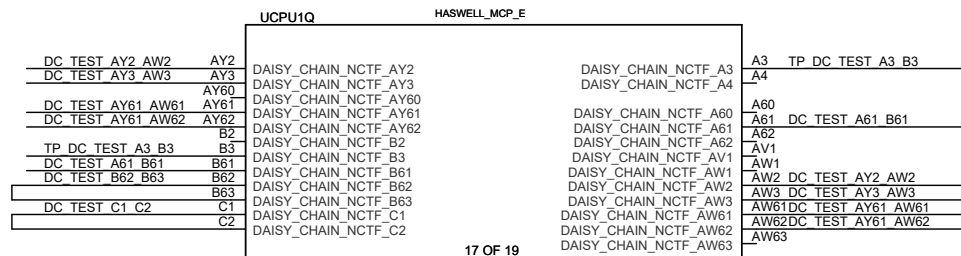
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Title		GPIO,UART,I2C	
Document Number	LA-A992P	Rev 0.1	
Date:	Thursday, March 20, 2014	Sheet	9 of 54

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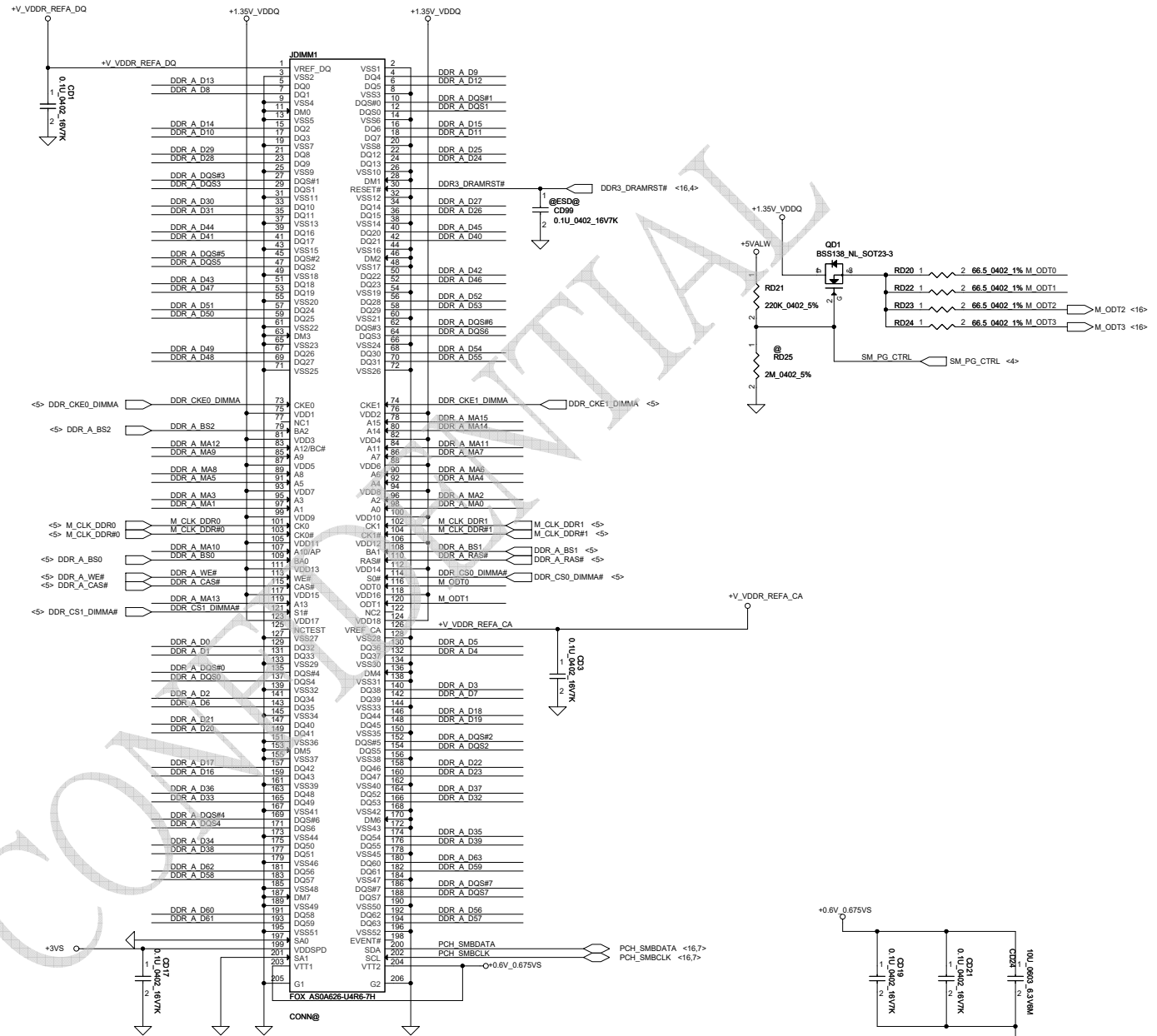


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/05/27	Deciphered Date	2011/05/11	Title	GND/VSSSEN
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				Date	Thursday, March 20, 2014
				Sheet	13 of 54



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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	RSVD/CFG
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Date:	Thursday, March 20, 2014	Sheet	14	of	54

<5> DDR_A_D[0..63]
 <5> DDR_A_DQS[0..7]
 <5> DDR_A_DQS#0..7
 <5> DDR_A_MA[0..15]



CONFIDENTIAL

RD9
1.8K_0402_1%

2

+1.35V_VDDQ

RD13
1.8K_0402_1%

1

2

RD17
1.8K_0402_1%

1

2

0.0220_0402_25V7K

RD12
24.9_0402_1%

2

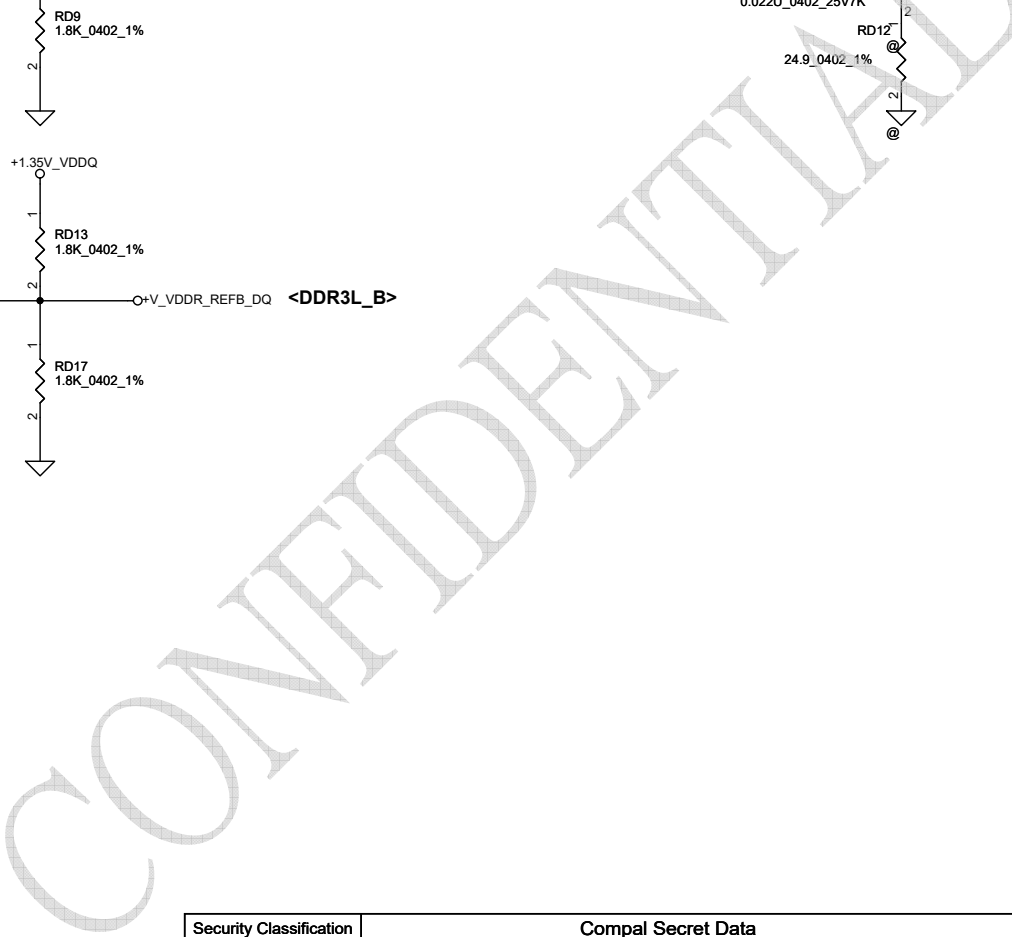
@

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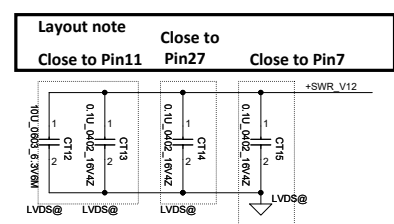
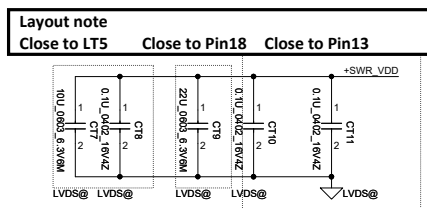
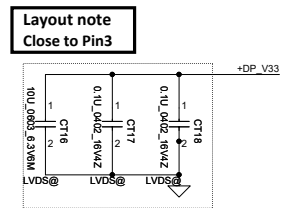
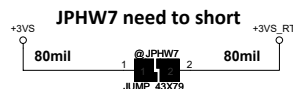
0+V_VDDR_REFB_DQ <DDR3L_B>

Security Classification

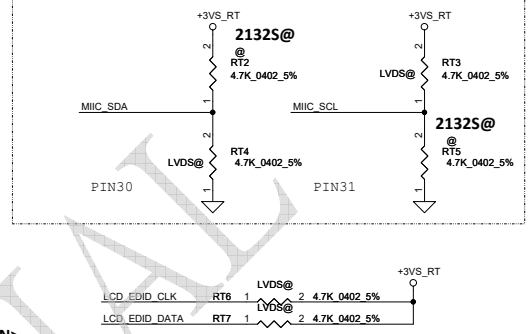
Compal Secret Data



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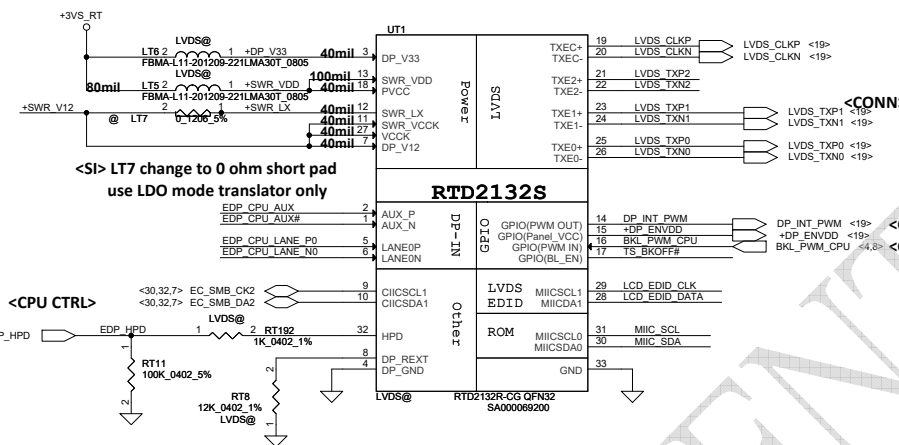
✱ ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.
EP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.
EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.
< ✱ Default mode >



SWR / LDO Mode select

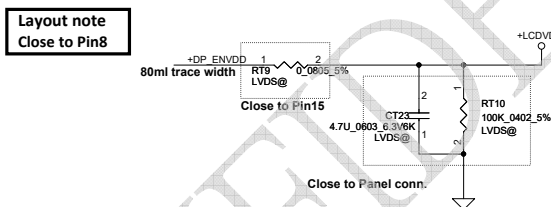
	LDO	SWR
2132S	Do not support	mount LT7
2132R	Use 0 ohm	mount LT7

✱ If use 2132R, please select LDO mode as default.



<CPU>

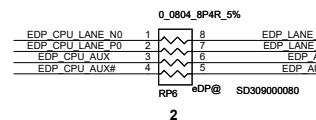
<4> EDP_CPU_AUX_C	CC102	1	2	.1U_0402_16V7K	EDP_CPU_AUX
<4> EDP_CPU_AUX#_C	CC101	1	2	.1U_0402_16V7K	EDP_CPU_AUX#
<4> EDP_CPU_LANE_P0_C	CC98	1	2	.1U_0402_16V7K	EDP_CPU_LANE_P0
<4> EDP_CPU_LANE_N0_C	CC97	1	2	.1U_0402_16V7K	EDP_CPU_LANE_N0



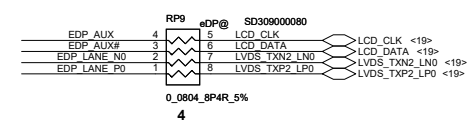
Different between 2132S and 2132R

2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

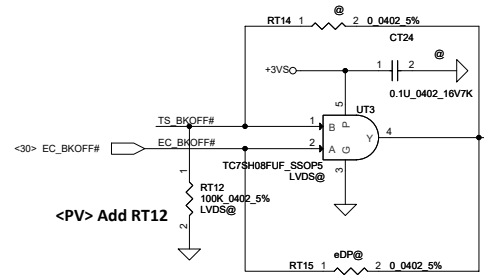
<CPU by PASS eDP>



<eDP to connector>



<RTS2132>
<EC CTRL>

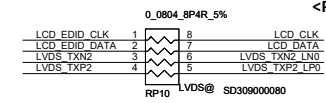


<Si> Update UT3 footprint (As UV11)

<LVDS Panel>

PD 100K on LVDS page

<LVDS to connector>



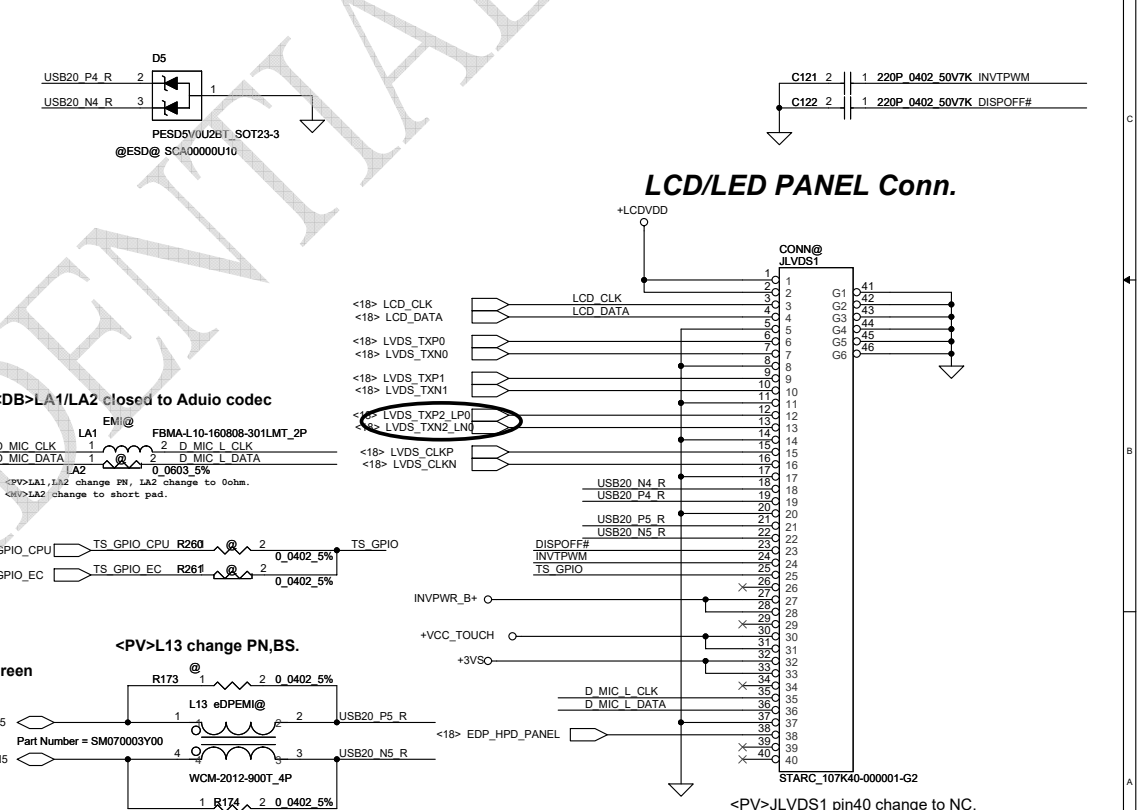
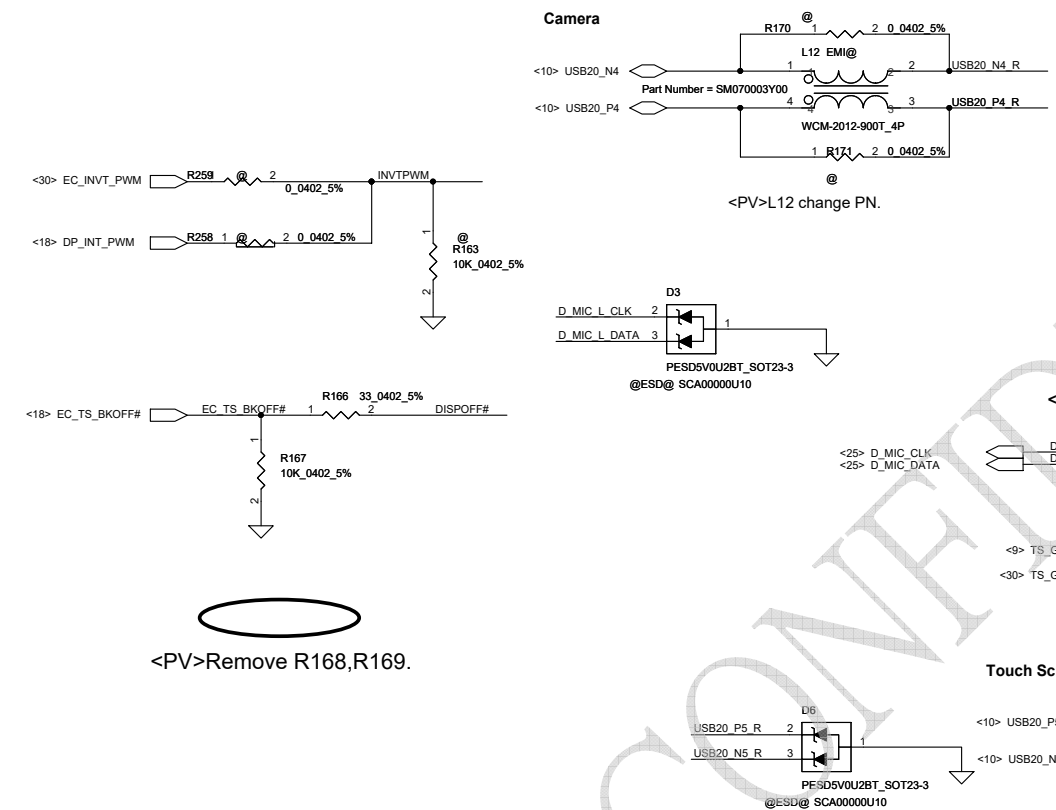
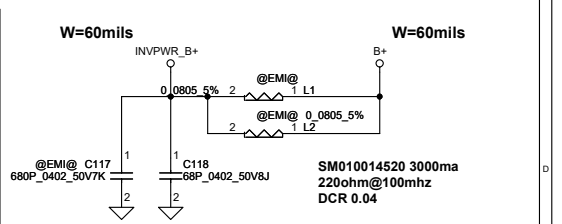
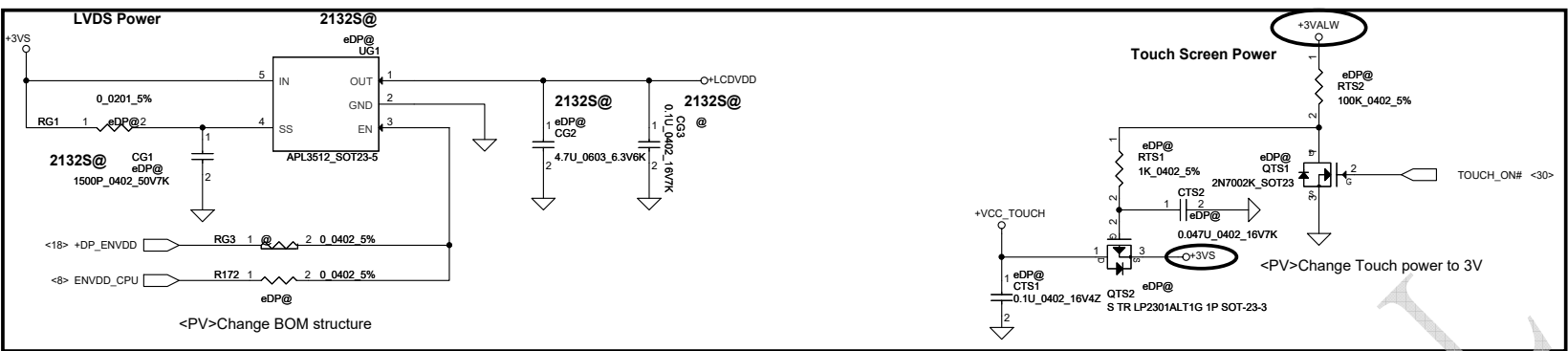
<PV>Change PR37 pin define , Add PR38.

<PV>PR36 Change to RP6.

PR37 change to RP9.

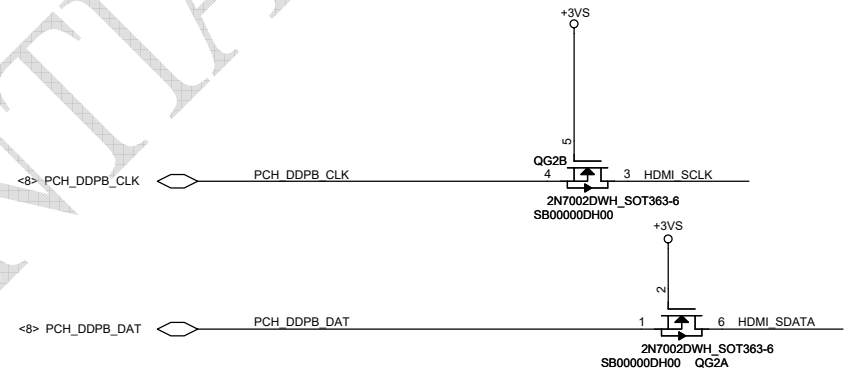
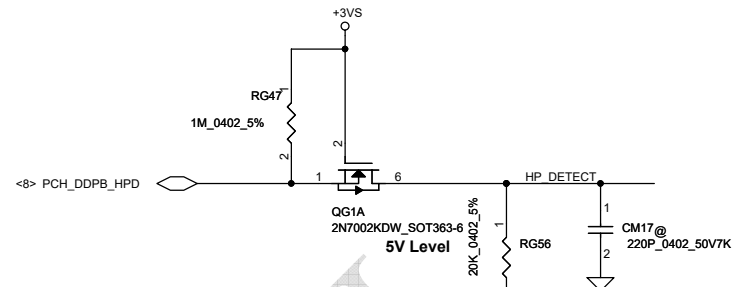
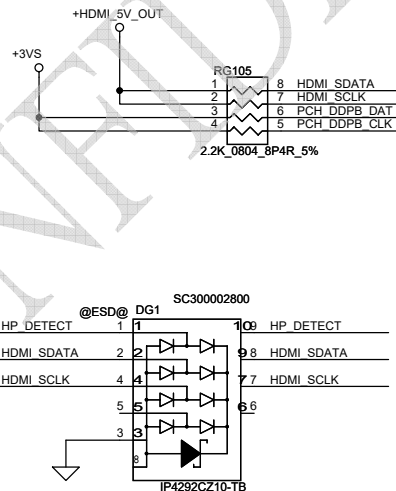
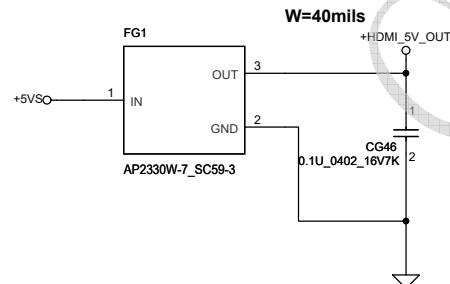
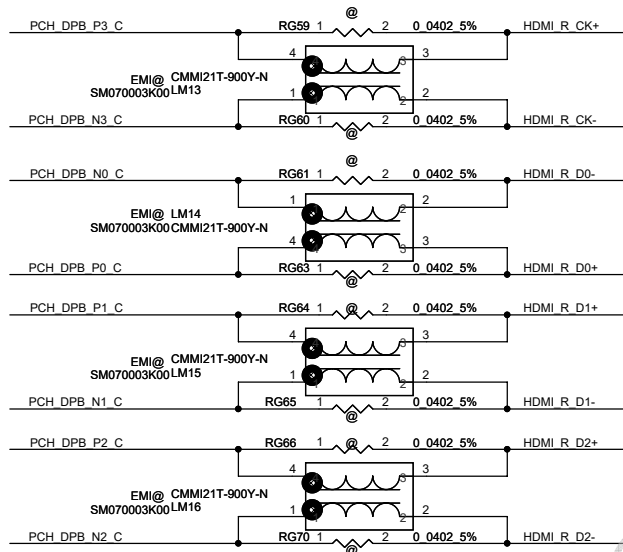
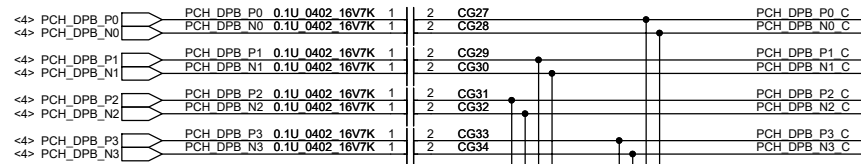
PR38 change to RP10.

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				LVDS Translator-RTD2132R
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				LA-A992P
Date: Thursday, March 20, 2014				Sheet 18 of 54

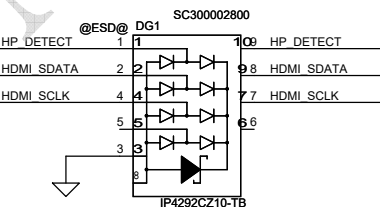
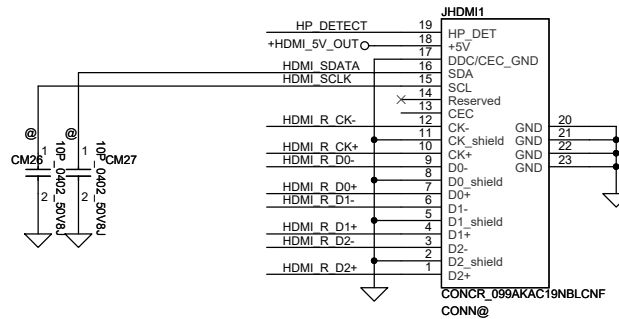


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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Rev
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Document Number				LA-A992P
Date:				Thursday, March 20, 2014
Sheet				19 of 54

<CPU>

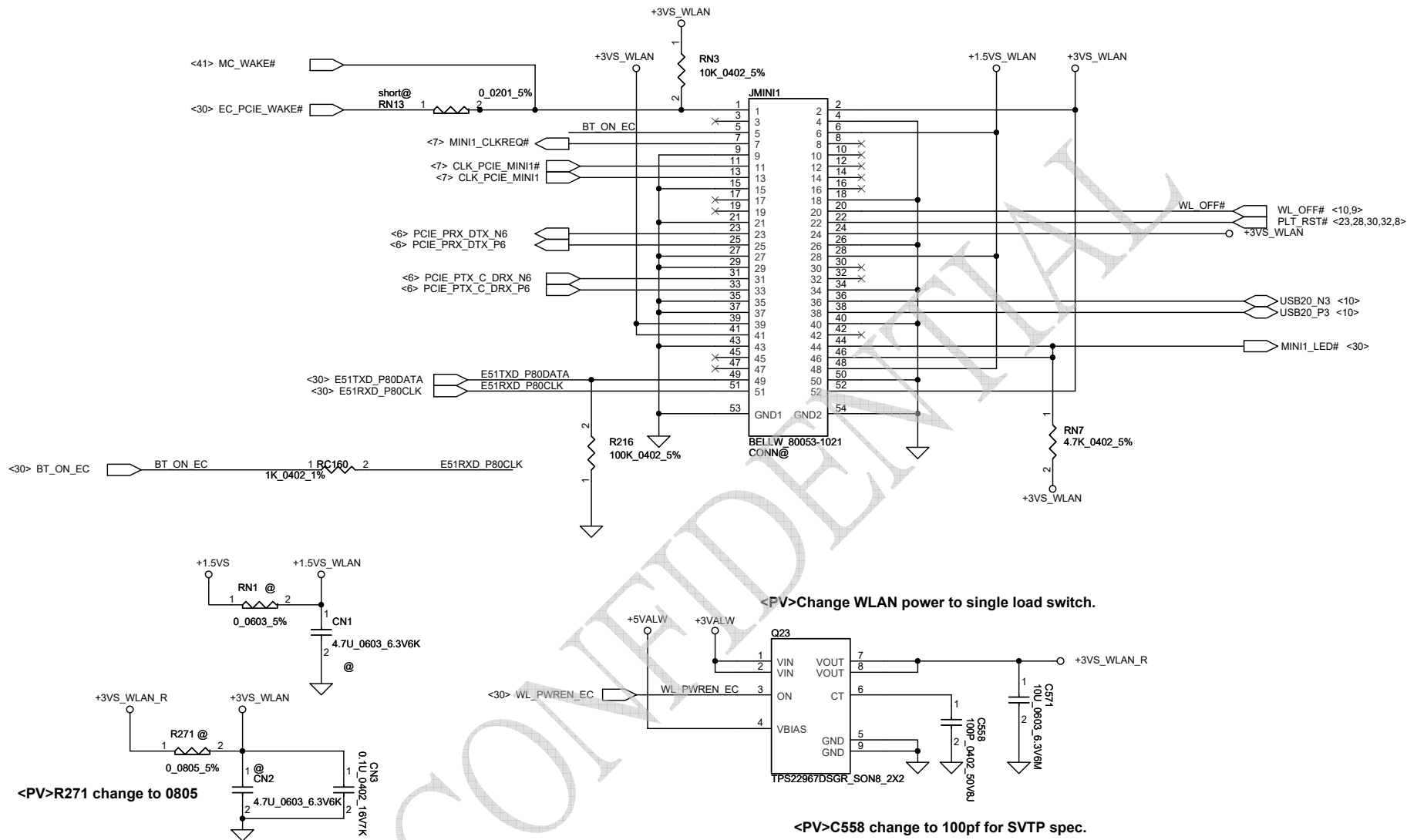


HDMI Conn.



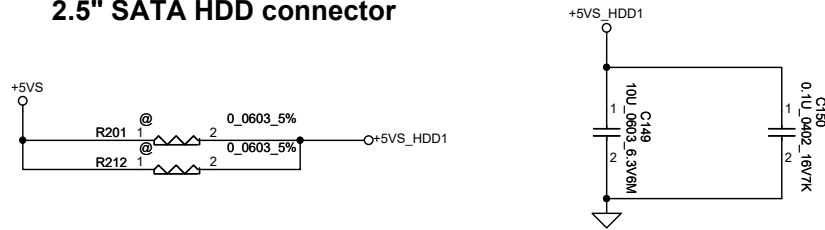
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	HDMI Conn/Level shift
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				Date	Thursday, March 20, 2014
				Sheet	20 of 54

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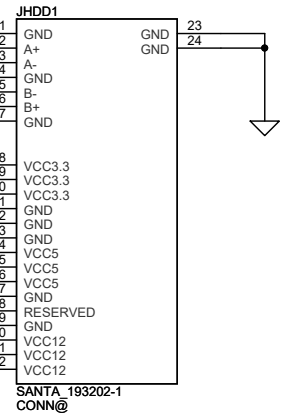
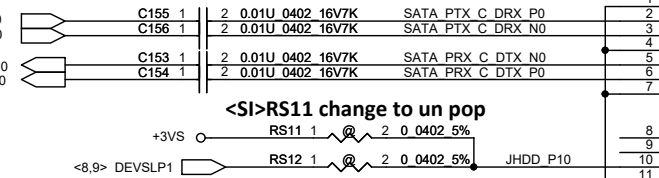


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				Date:	Thursday, March 20, 2014
				Sheet	21 of 54

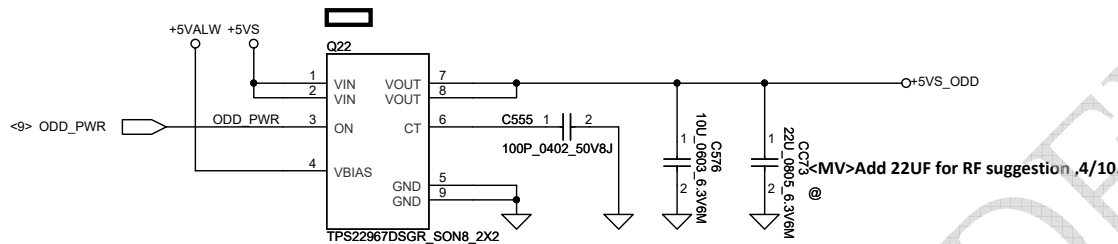
2.5" SATA HDD connector



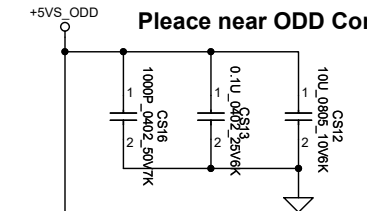
<6> SATA_PTX_DRX_P0
<6> SATA_PTX_DRX_N0
<6> SATA_PRX_DTX_N0
<6> SATA_PRX_DTX_P0



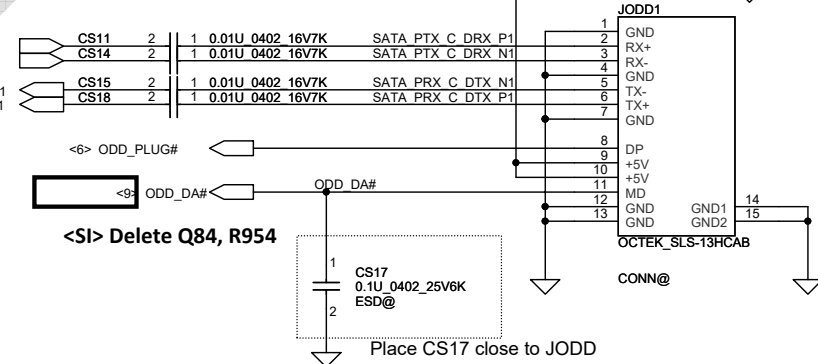
Change to dual load switch for ODD and WLAN
<PV>Q22 change to single load switch.



Place near ODD Connector



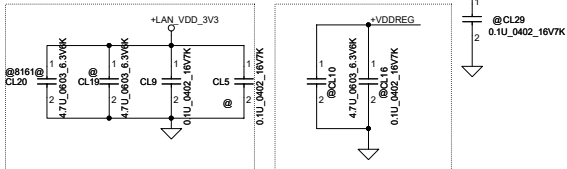
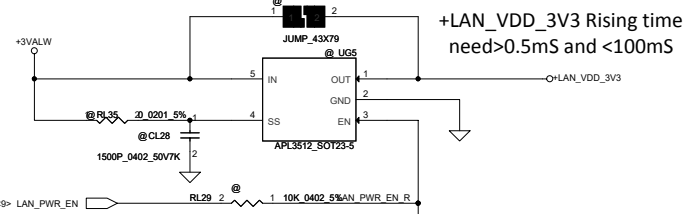
<6> SATA_PTX_DRX_P1
<6> SATA_PTX_DRX_N1
<6> SATA_PRX_DTX_N1
<6> SATA_PRX_DTX_P1



Place CS17 close to JODD

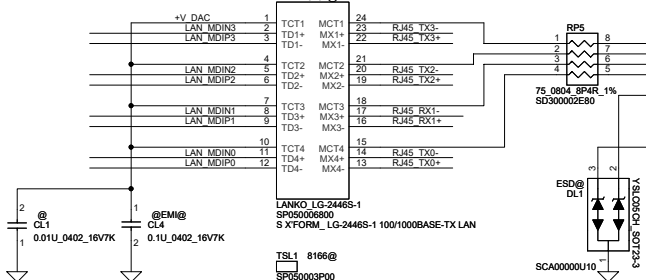
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	ODD/SATA Conn
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				Date:	Thursday, March 20, 2014
				Sheet	22 of 54

JHW1 need to short



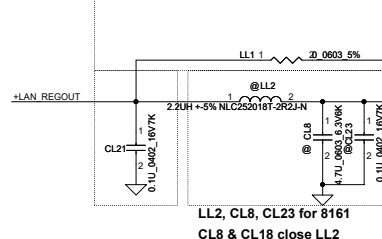
CL9 & CL5 close to UL1: Pin 11,32
CL19 close to UL1: Pin 32
CL20 close to UL1: Pin 11

SP050005L00 Footprint

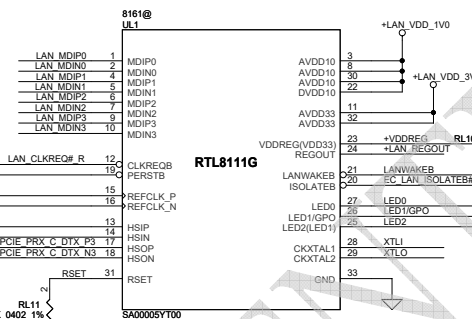


SP050005L00
S XFORM_LG-2446S-1 100/1000BASE-TX LAN
(SP050003P00) 10/100 8166@
(SP050006800) Giga 8161@

RTL8151G (LDO mode)



8151/8166 Co-Lay



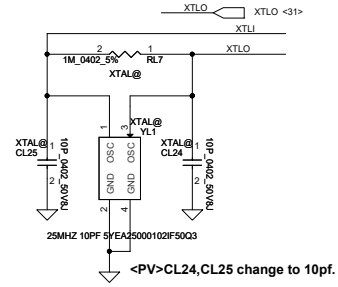
(SA000063500) 10/100 8166@
(SA00005YT00) Giga 8151@

	LDO mode	Switching mode
LL1	SMT	@
CL21	SMT	@
LL2	@	SMT
CL8	@	SMT

CL14 & CL15 close UL1 Pin22
CL26 & CL27 close UL1 Pin30

Place CL11-CL13 close UL1 Pin 3, 8, 22

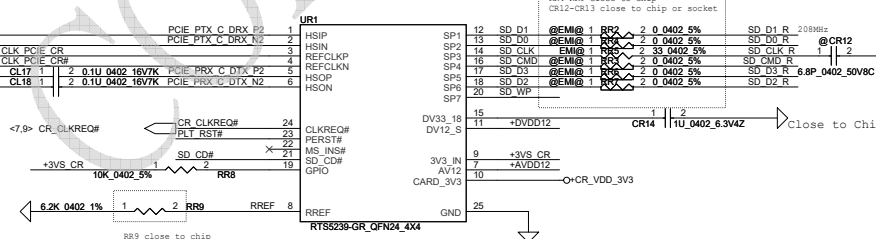
+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil



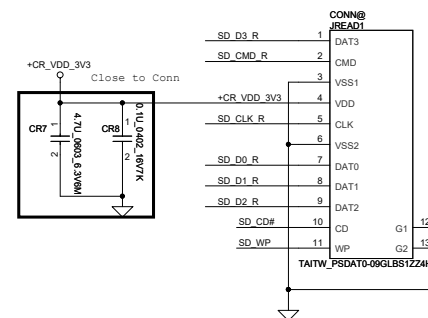
<PV>CL24,CL25 change to 10pf.

SANTA 130456-291 JLAN1 CONN@	
RJ45 TX3-	8
RJ45 TX3+	7
RJ45 RX1-	6
RJ45 TX2-	5
RJ45 TX2+	4
RJ45 RX1+	3
RJ45 TX0-	2
RJ45 TX0+	1

RTS5239

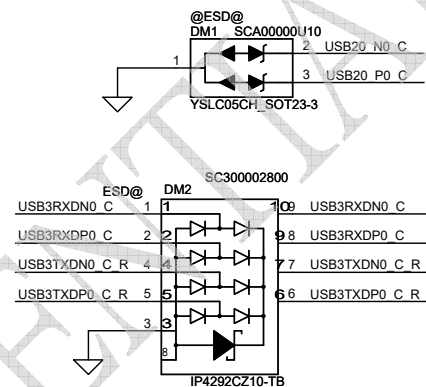
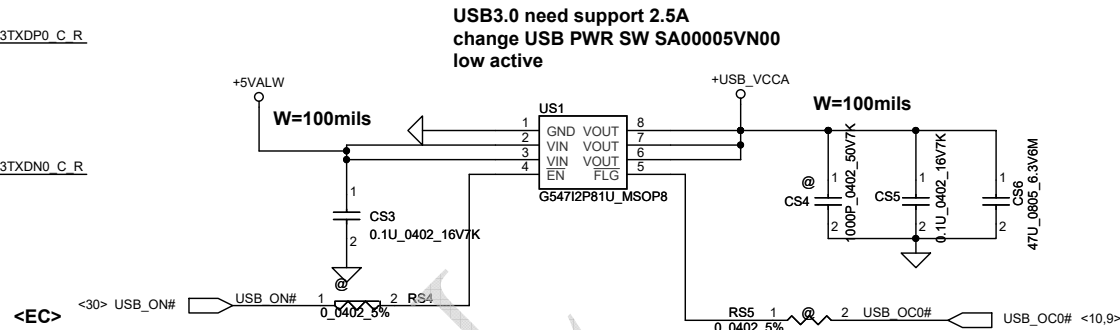
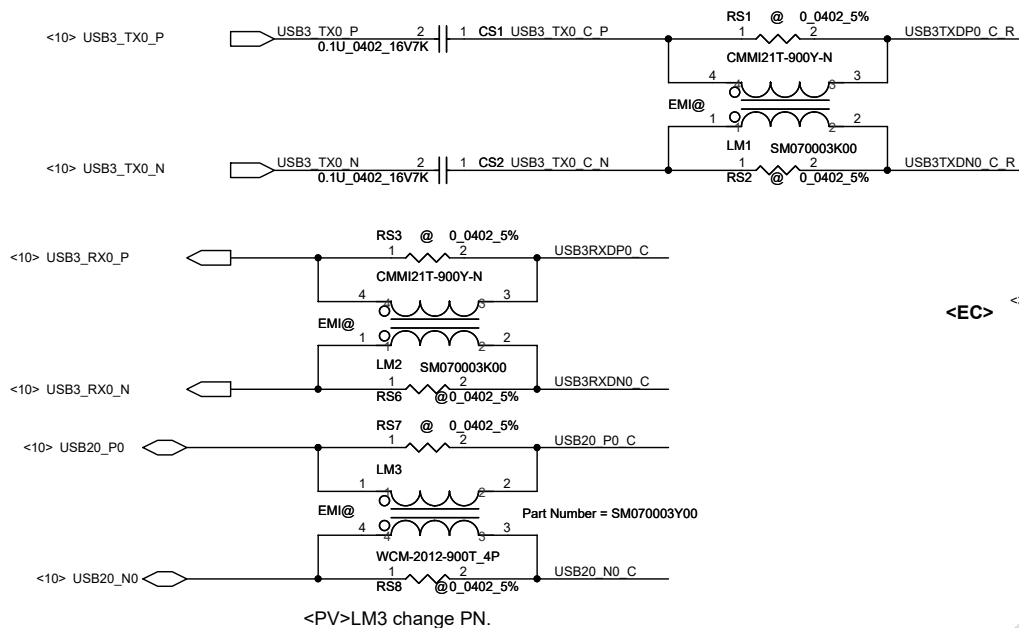


Card Reader Connector

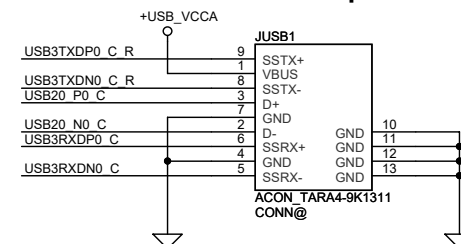


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Issued Date	2013/02/26	Deciphered Date
2015/07/08		
Title		LAN 8111G
Size	Document Number	LA-A992P
Date	Thursday, March 20, 2014	Sheet 23 of 54

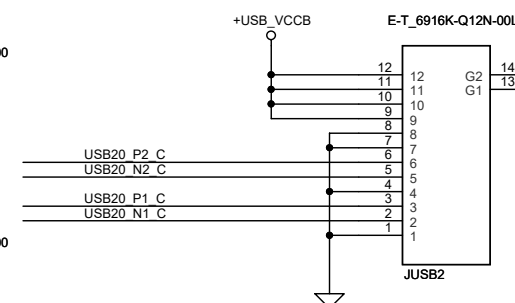
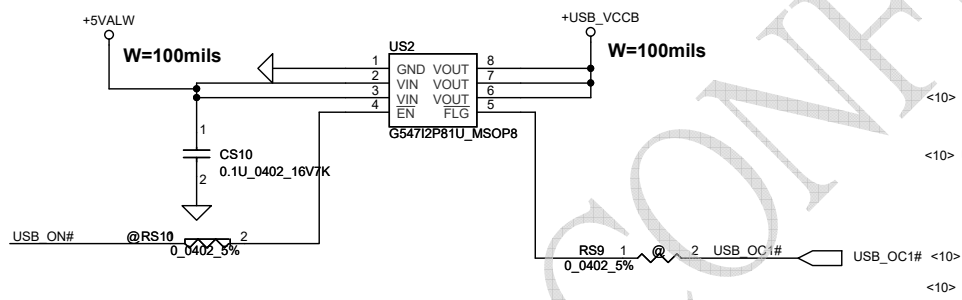
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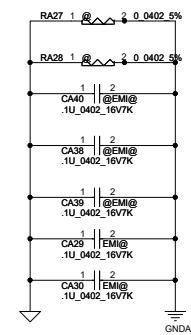
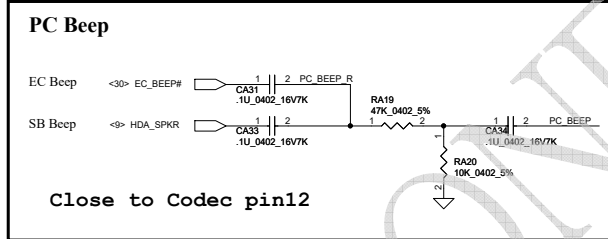
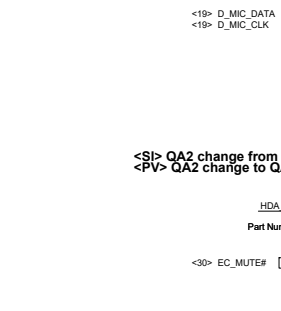
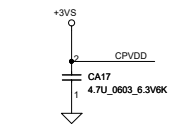
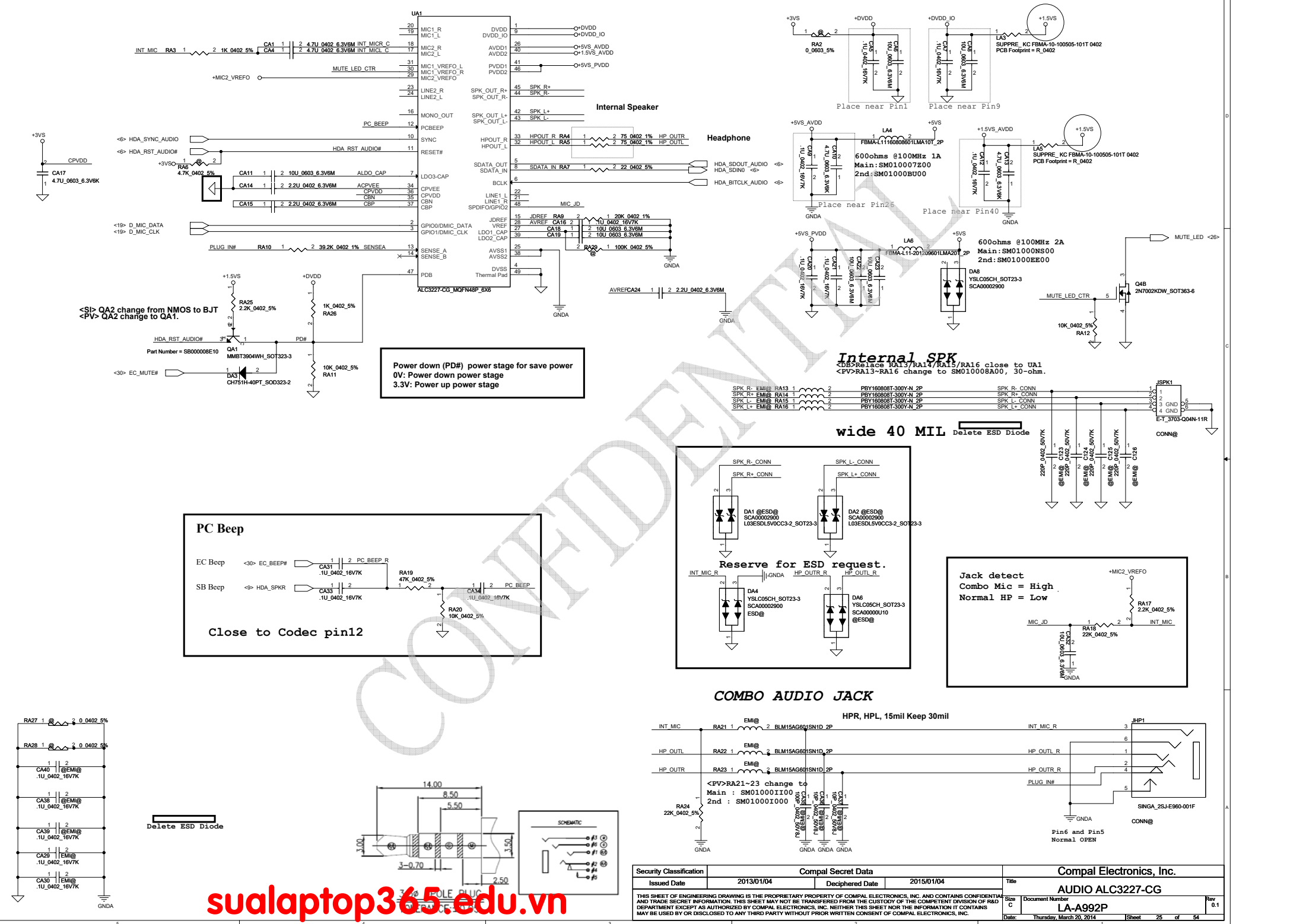
USB2.0/USB3.0 port 1



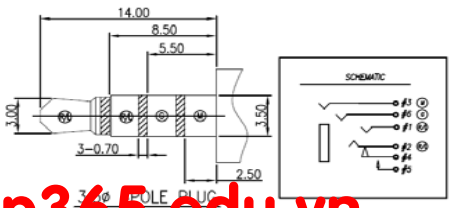
USB2.0 port x 2



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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	USB 3.0/2.0 conn
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				Date:	Thursday, March 20, 2014
				Sheet	24 of 54



Delete ESD Diode



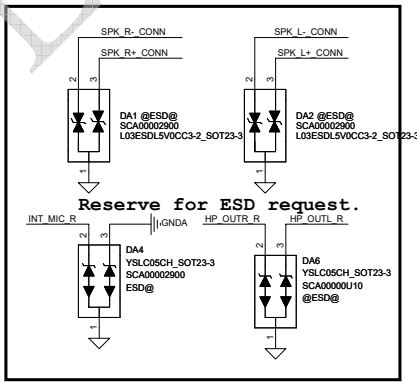
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Internal Speaker

Headphone

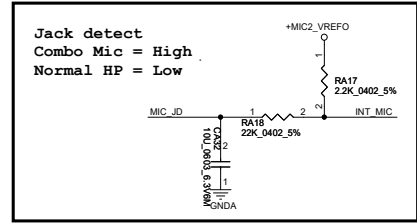
Internal SPK

wide 40 MIL Delete ESD Diode



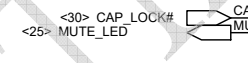
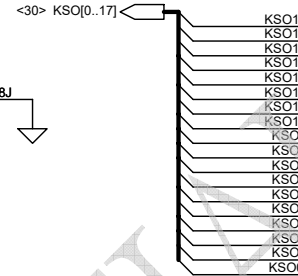
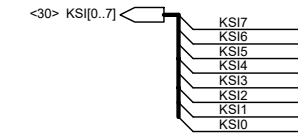
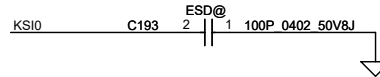
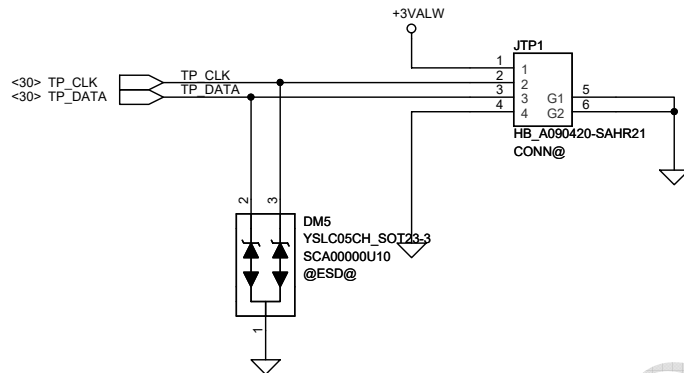
COMBO AUDIO JACK

HPR, HPL, 15mil Keep 30mil

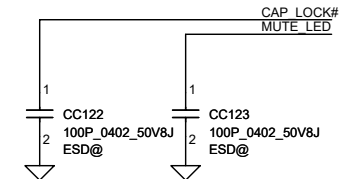
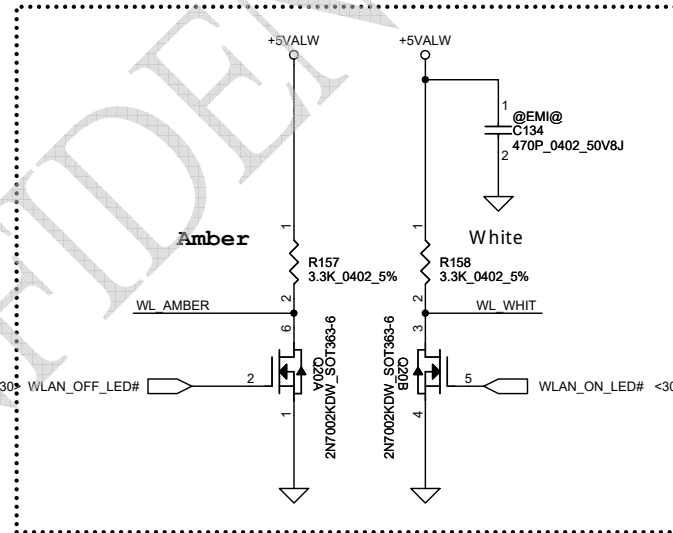
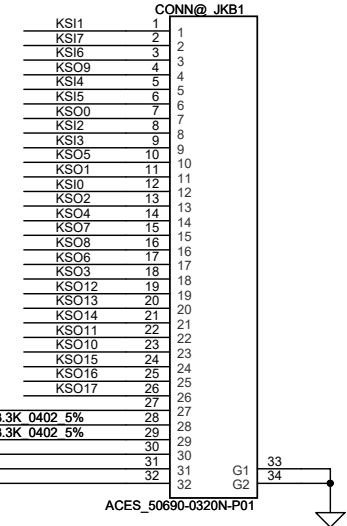


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Issued Date	2013/01/04	Deciphered Date	2015/01/04	Title	AUDIO ALC3227-CG
Size C		Document Number	LA-A992P	Rev	0.1
Date		Thursday, March 20, 2014	Sheet	25	of 54

Touch pad conn

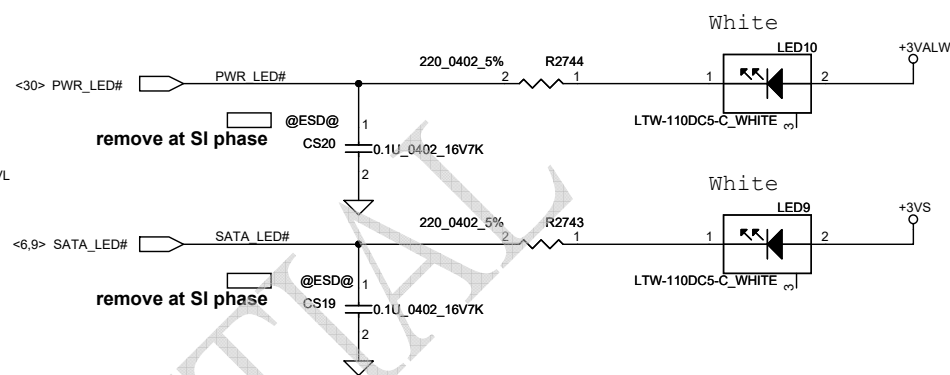
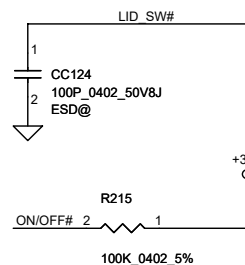
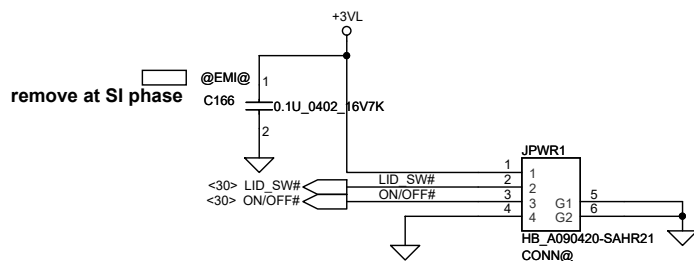


Keyboard conn

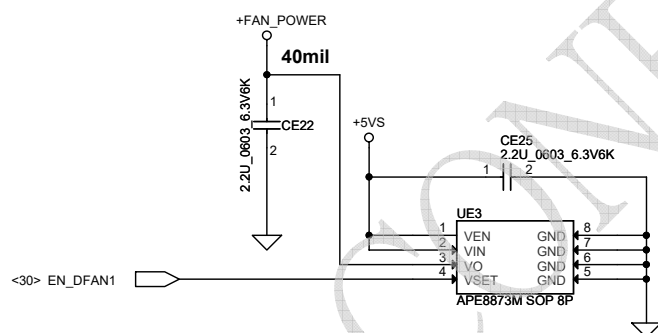


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								KB/TP			
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								LA-A992P		0.1	
								Date: Thursday, March 20, 2014		Sheet 26 of 54	

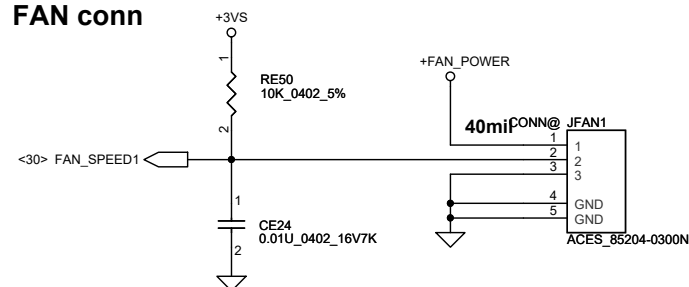
Power Button Connector



<SI> Del New Lid SW conn

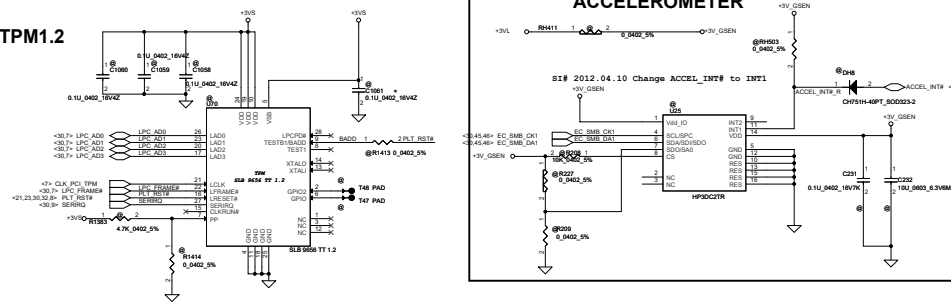


FAN conn

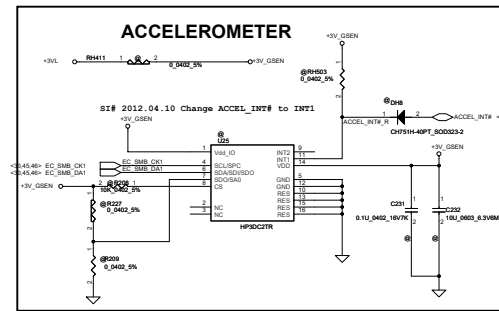


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Date				Thursday, March 20, 2014				Sheet 27 of 54			
Rev				0.1				LA-A992P			

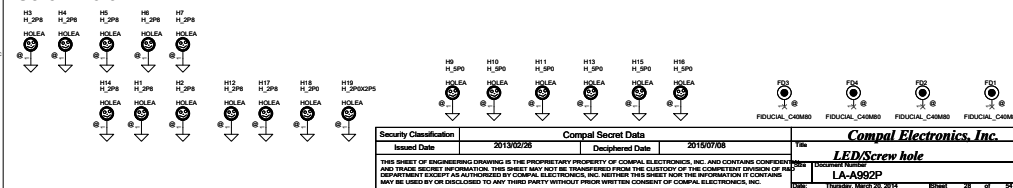
TPM1.2

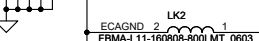
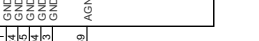
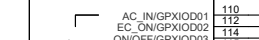
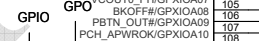
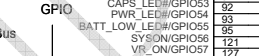
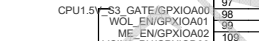
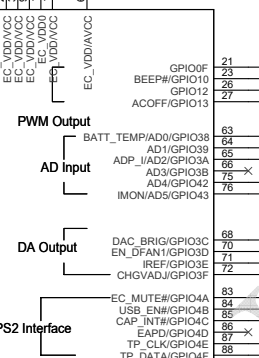
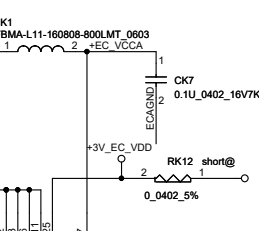
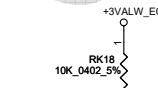
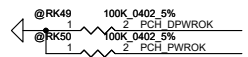
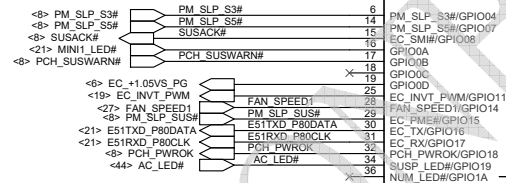
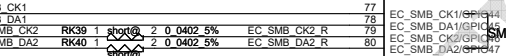
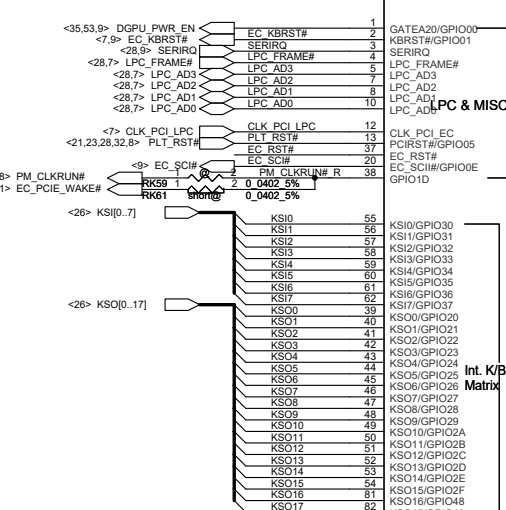
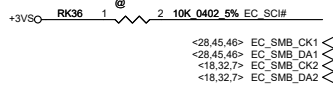
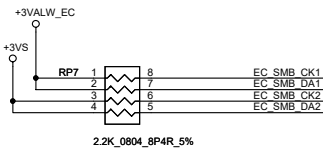


ACCELEROMETER



Screw Hole

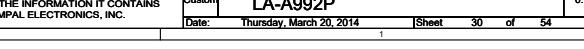
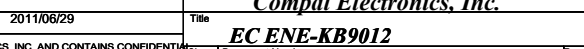
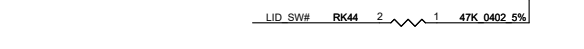
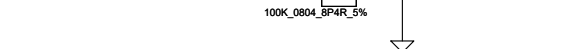
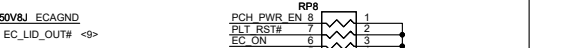
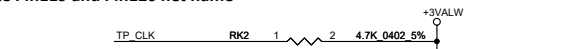
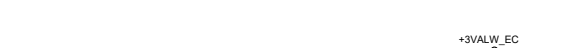
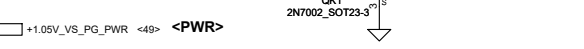
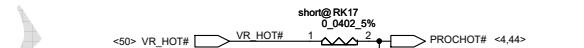
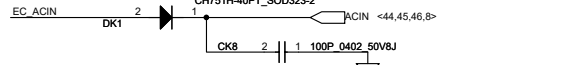




15"	<i>DB</i>	<i>SI</i>	<i>PV</i>	<i>MV</i>
<i>UMA</i> <i>RK13</i>	12k ohm	20K ohm	33K ohm	56K ohm
<i>DIS</i> <i>RK13</i>	160k ohm	240k ohm	330k ohm	560k ohm

Board ID control
 <DB>RK13 change to 160K ==>for 15" DIS
 <DB>RK13 change to 12K ==>for 15" UMA

$14''$	DB	SI	PV	MV
UMA $RK13$	$0\ ohm$	$15K\ ohm$	$27K\ ohm$	$43K\ ohm$
DIS $RK13$	$130k\ ohm$	$200k\ ohm$	$270k\ ohm$	$430k\ ohm$

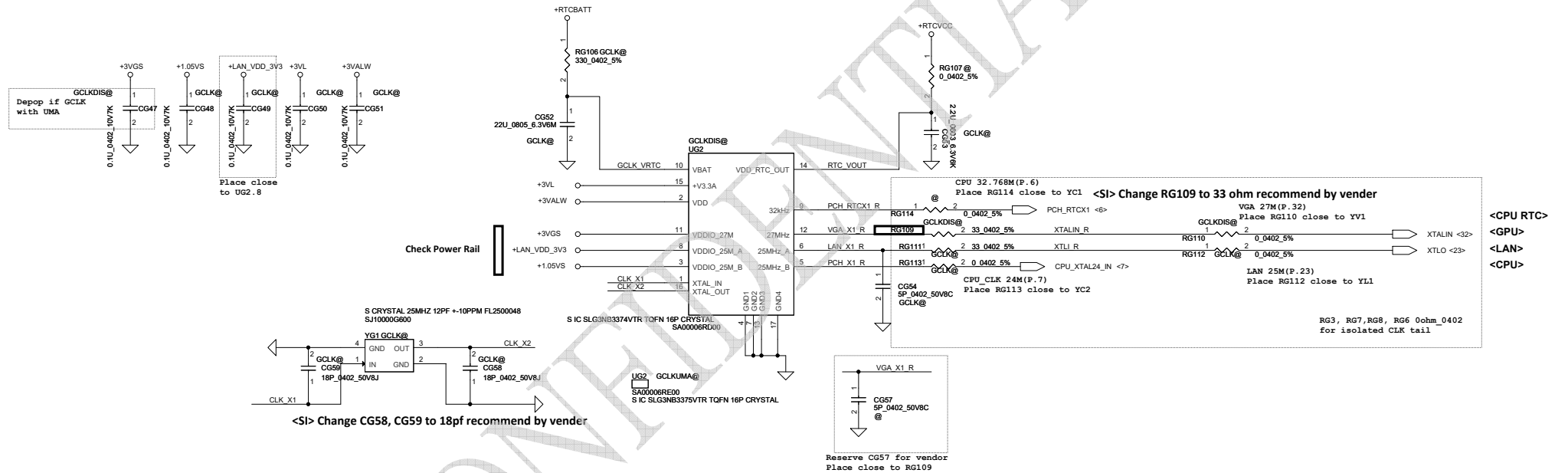


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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title		
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				Cust	LA-A992P	0.1
				Date:	Thursday, March 20, 2014	Sheet 30 of 54

BOM control

Platform	Silego P/N	Compal PN	25MHz(A)	32.768KHz	24MHz(B)	27MHz	8MHz	Remark
Intel ULT UMA	SLG3NB3375V	SA00006RE00	1	1	1	X	X	GCLKUMA@
Intel ULT Dis	SLG3NB3374V	SA00006RD00	1	1	1	1	X	GCLKDIS@

Base on A32 32.768KHz use 10ppm, G-CLK 25MHz X'TAL use 10ppm.



<CPU>

<CPU>

<CPU>

Differential signal

EC or CPU control

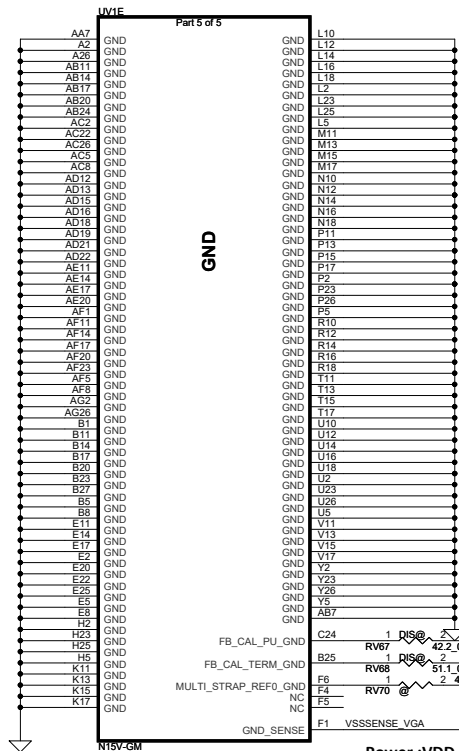
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#9/2 , Add RV191 between.
GPU_PWR_LEVEL# and GPU_THERMAL_DET#

#8/19 ,N15V-GM didn't support GC6,
unpop QV13 ,QV14.

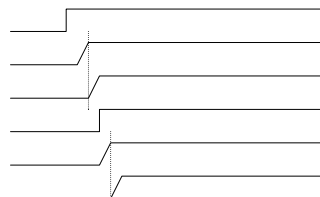
<PV>CV9,CV10 change to 10pf.

Security Classification		Compal Secret Data		Title	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	N15V-GM PCIE/DAC/GPIO	
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				Custom	LA-A992P
				Date:	Thursday, March 20, 2014
				Sheet	32 of 54

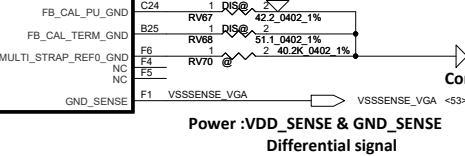


Power on

DGPU_PWR_EN
+3VGS
+VGA_CORE
DGPU_PWROK
+1.05VGS
+1.5VGS



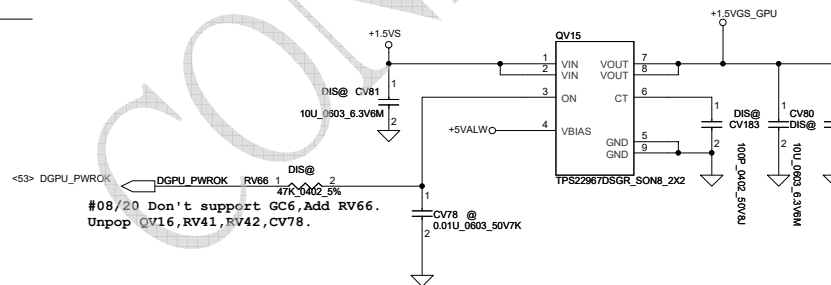
40us < Rt < 2ms



#8/19.RV70 unpop, N15V-GM use binary mode.
Contrl by power

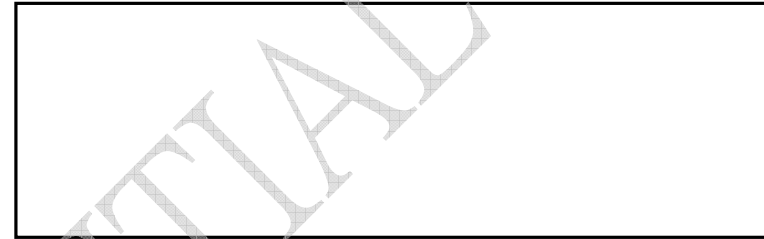
+1.5VGS=3.6A,8vias.

+1.5VGS_GPU
#8/19.QV15 change to TPS22967
+1.5V to +1.5VGS

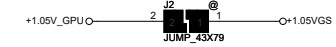


#08/20 Don't support GC6, Add RV66.
Unpop QV16, RV41, RV42, CV78.

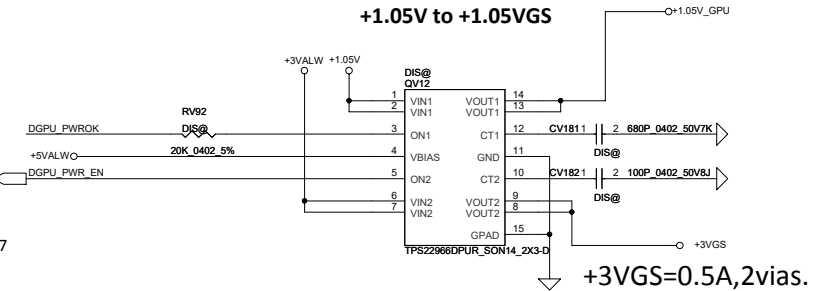
#8/20 : N15V-GM don't support GC6 function. UV20 unpop.



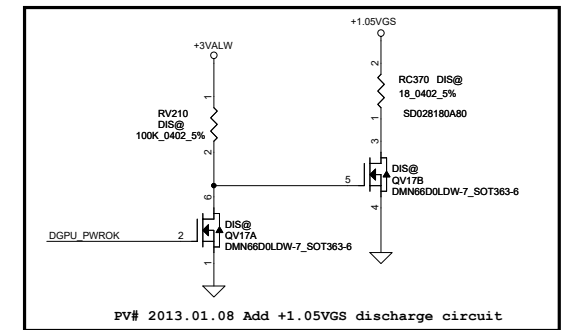
+1.05VGS=1.6A,4vias.



+3VALW to +3VGS
+1.05V to +1.05VGS

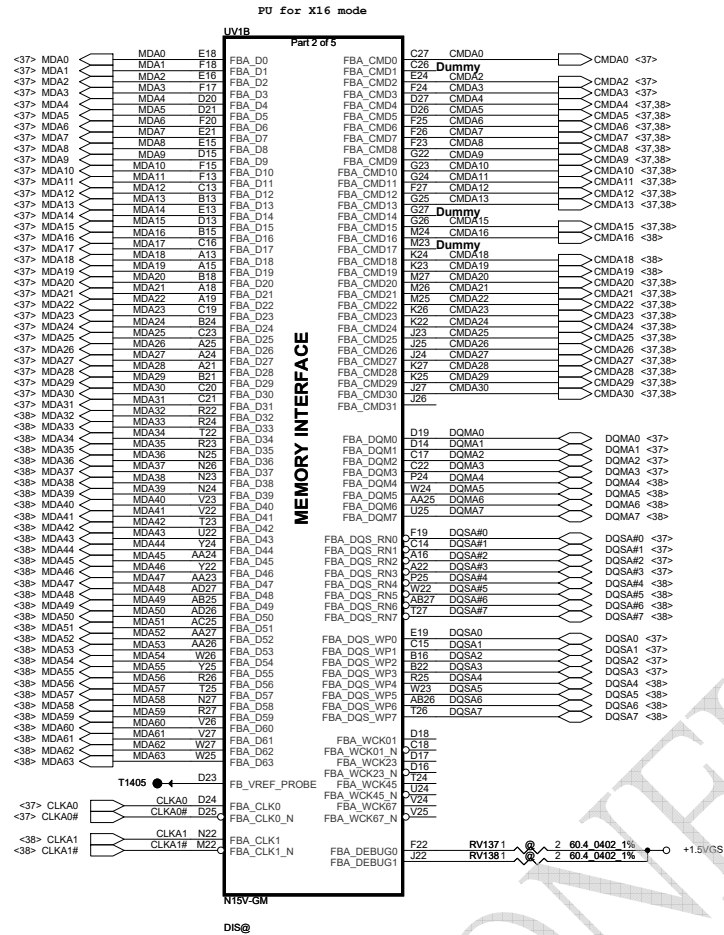


+3VGS=0.5A,2vias.

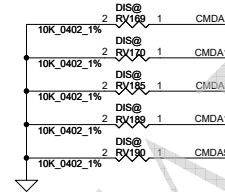


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				Rev	0.1
				Date	Thursday, March 20, 2014
				Sheet	35 of 54



Note: DG use 1%



Mode D Command Mapping

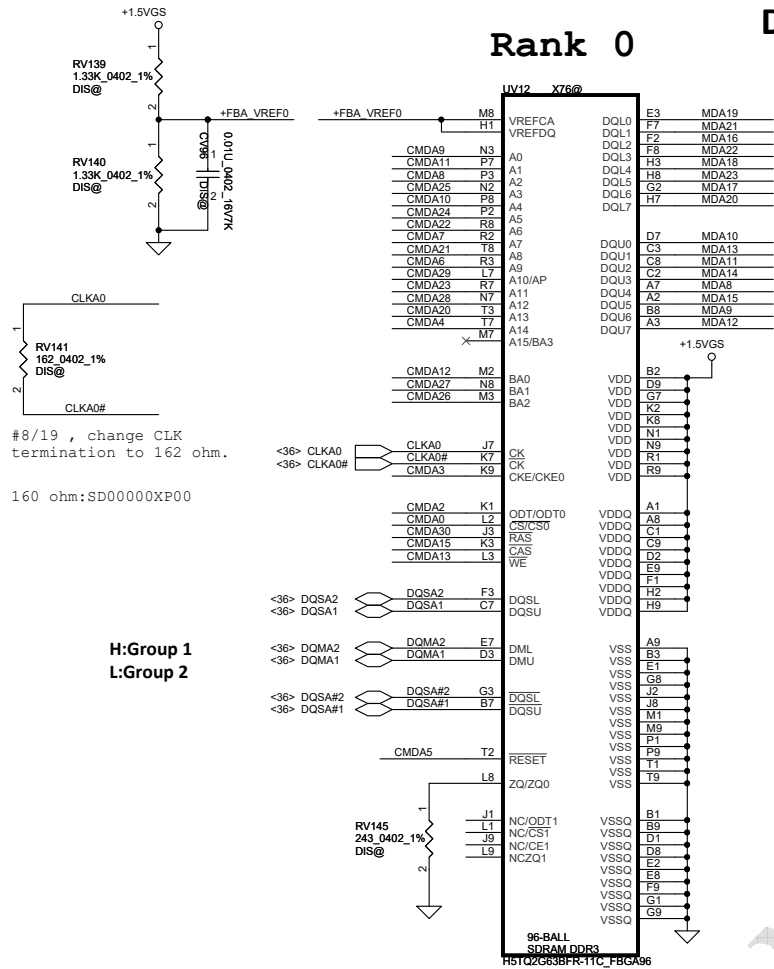
Address	RANK 0	
	0..31	32..63
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14		
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#
FBx_CMD17		
FBx_CMD18	ODT	
FBx_CMD19	CKE	
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Memory Partition A RANK 0

Data0~Data31

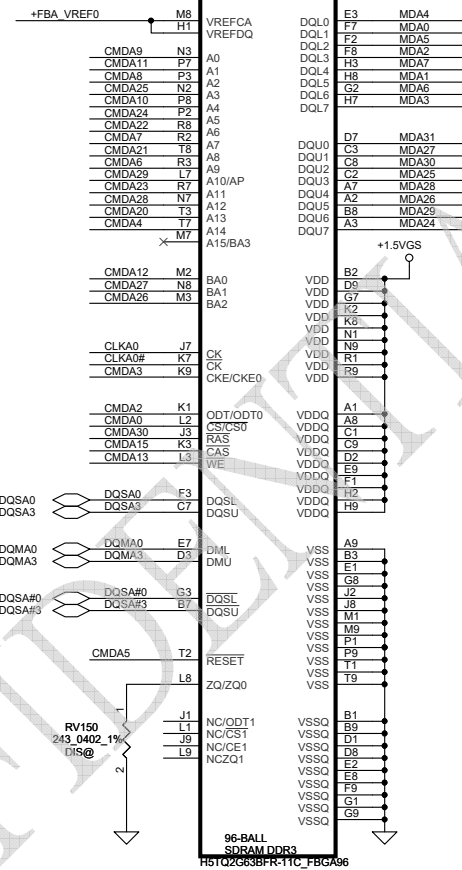
Rank 0

Rank 0



Group 2

Group 1

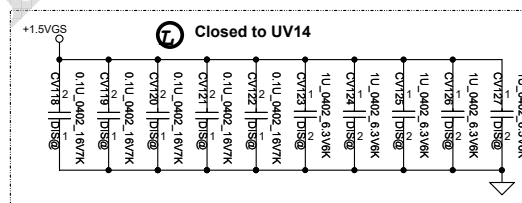
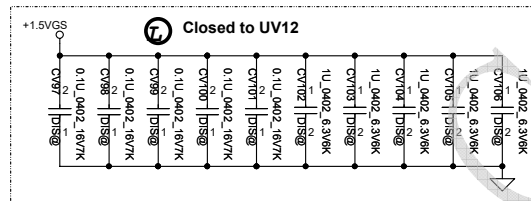
L:Group 0
H:Group 3

Group 0

Group 3

Mode D Command Mapping

RANK 0		
Address	0..31	32..63
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14		
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



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				Date	Thursday, March 20, 2014
				Sheet	37 of 54

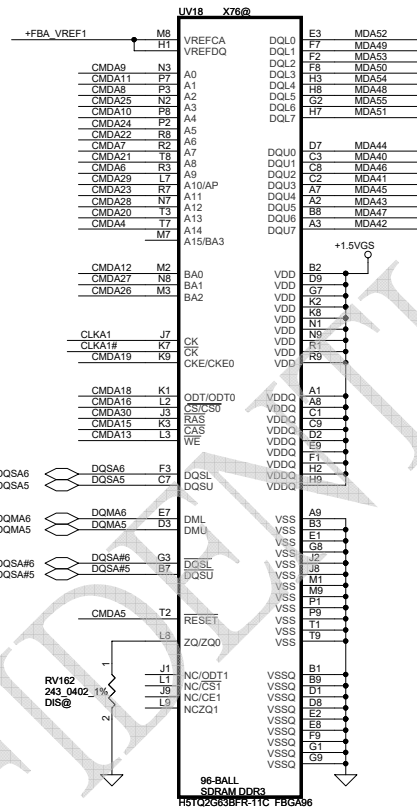
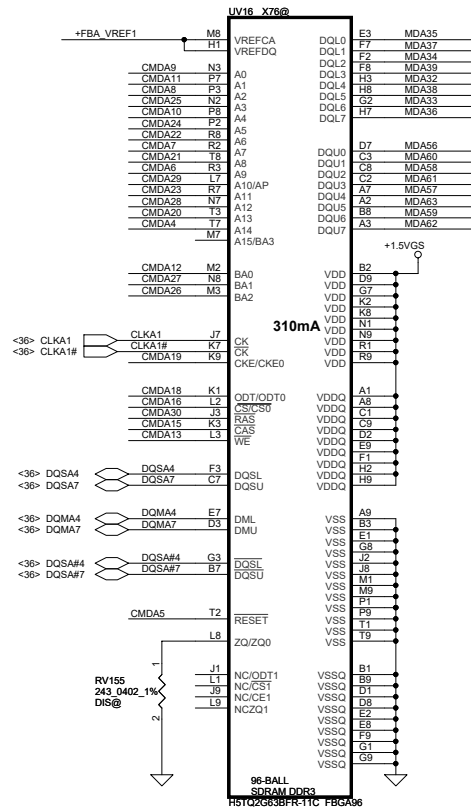
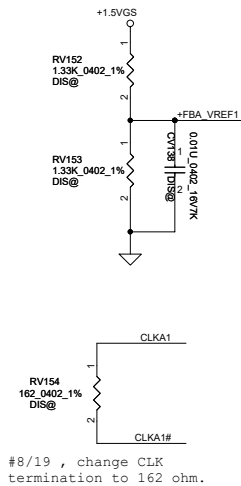
Memory Partition A RANK 0 32 bits

Rank 0

Data32~Data63

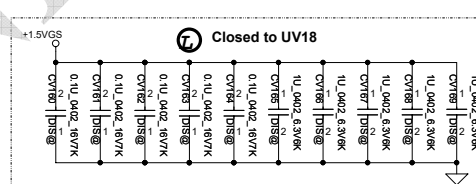
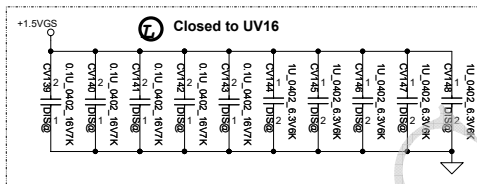
Rank 0

MDA[0..63] <36,37>
CMDA[90..0] <36,37>



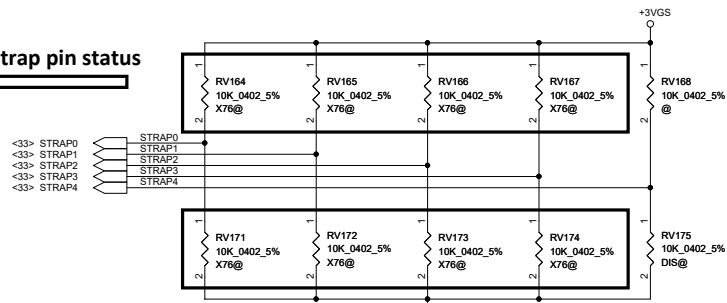
Mode D Command Mapping

Address	0..31	32..63
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14		
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
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FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

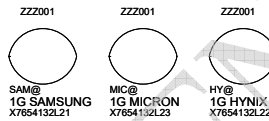
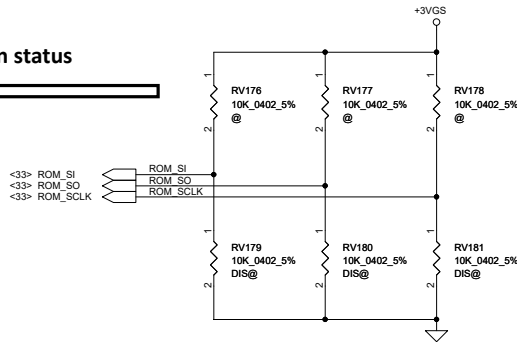


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Date	Thursday, March 20, 2014	Sheet	38 of 54

Check Strap pin status



Check SPI pin status



GPU	Project	VRAM size	CH	Description	Compal VRAM P/N	VRAM description	ROM CFG setup [3...0]	RAM_CFG	R P/N
N15V-GM (23x23) 64bit (One CH single rank)	ZSO40	128M(X16)	CHA	DDR3 Hynix 128Mx16 1.5V	SA00006H400	H5TC2G63FFR-11C 1000MHz	1100	RV171+RV172+RV167+RV166	
	ZSO50	128M(X16)	CHA	DDR3 Micron 128Mx16 1.5V	SA000067500	MT41J128M16JT-093G-K 1000MHz	0001	RV164+RV172+RV173+RV174	
		128M(X16)	CHA	DDR3 Samsung 128Mx16 1.5V	SA000068U40	K4W2G1646Q-BC1A 1000MHz	1110	RV165+RV166+RV167+RV171	

#9/5 RAM_CFG follow RVL-06891-001 table 1.
Dule Rank layout with single Rank population.

Table 123

Strap pin Name	Strap Mapping	Resistance	Polarity	Logical Strapping Bit0
ROM_SCLK	SMB_ALT_ADDR	10K	Pull-down to GND.	
ROM_SI	SUB_VENDOR	10K	Pull-down to GND if no VBIOS ROM.	
ROM_SO	VGA_DEVICE	10K	Pull-down to GND(no diaplay).	
STRAP0	RAM_CFG[0]	10K		
STRAP1	RAM_CFG[1]	10K		
STRAP2	RAM_CFG[2]	10K		
STRAP3	RAM_CFG[3]	10K		
STRAP4	PCIE_MAX_SPEED	10K	Pull-down to GND(PCIE Gen1).	

SMBUS_ALT_ADDR

0	0x9E (Default)
1	0x9C (Multi-GPU usage)

SUB_VENDOR

0	Disable (Default)
1	

VGA_DEVICE

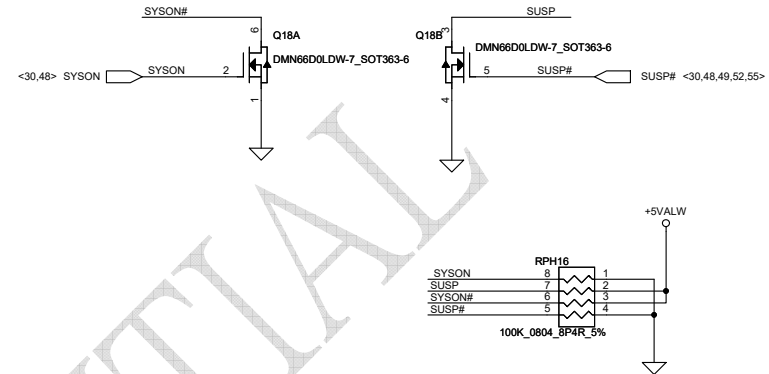
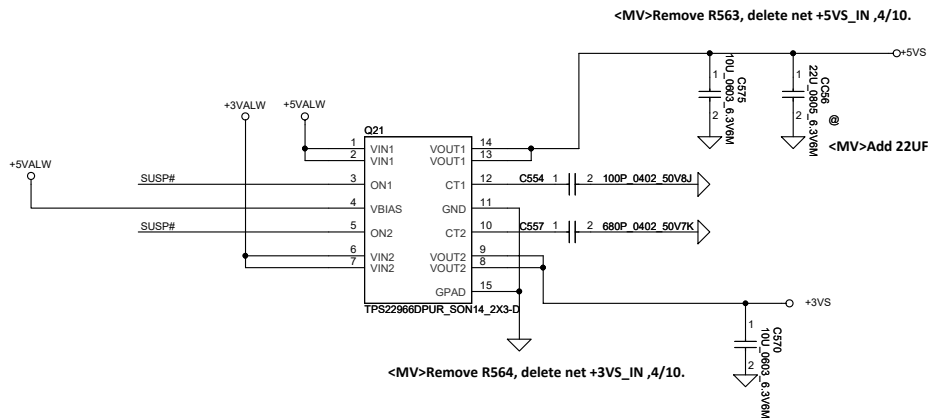
0	Non-Primary 3D Acceleration Device(Class Code 302h)(Default)
1	Primary Display or VGA Device .

PCIE_MAX_SPEED

0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

USER Straps

User[3:0]	
1000-1100	Customer defined

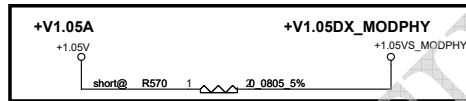


+1.05V TO +1.05VS



AO4430L
VGS Max=+/- 20V
VGS(Th) max=2.5V

Rds Max=5.5m @VGS=10V
Rds Max=7.5m @VGS=4.5V

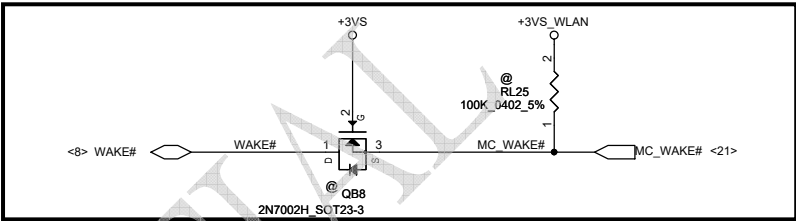


CPU +V1.05DX_MODPHY
Max Rdson <6m ohm
1840mA

AO4430L
VGS Max=+/- 20V
VGS(Th) max=2.5V
Rds Max=5.5m @VGS=10V
Rds Max=7.5m @VGS=4.5V

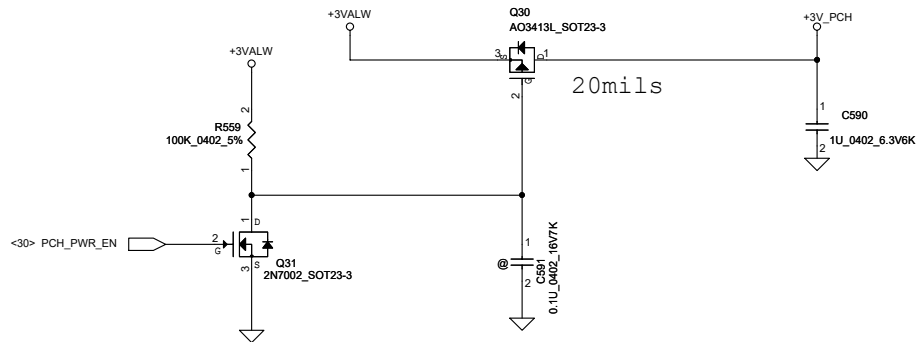
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								DC Interface			
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						Date:		Thursday, March 20, 2014		Sheet 40 of 54	

NGFF and WLAN



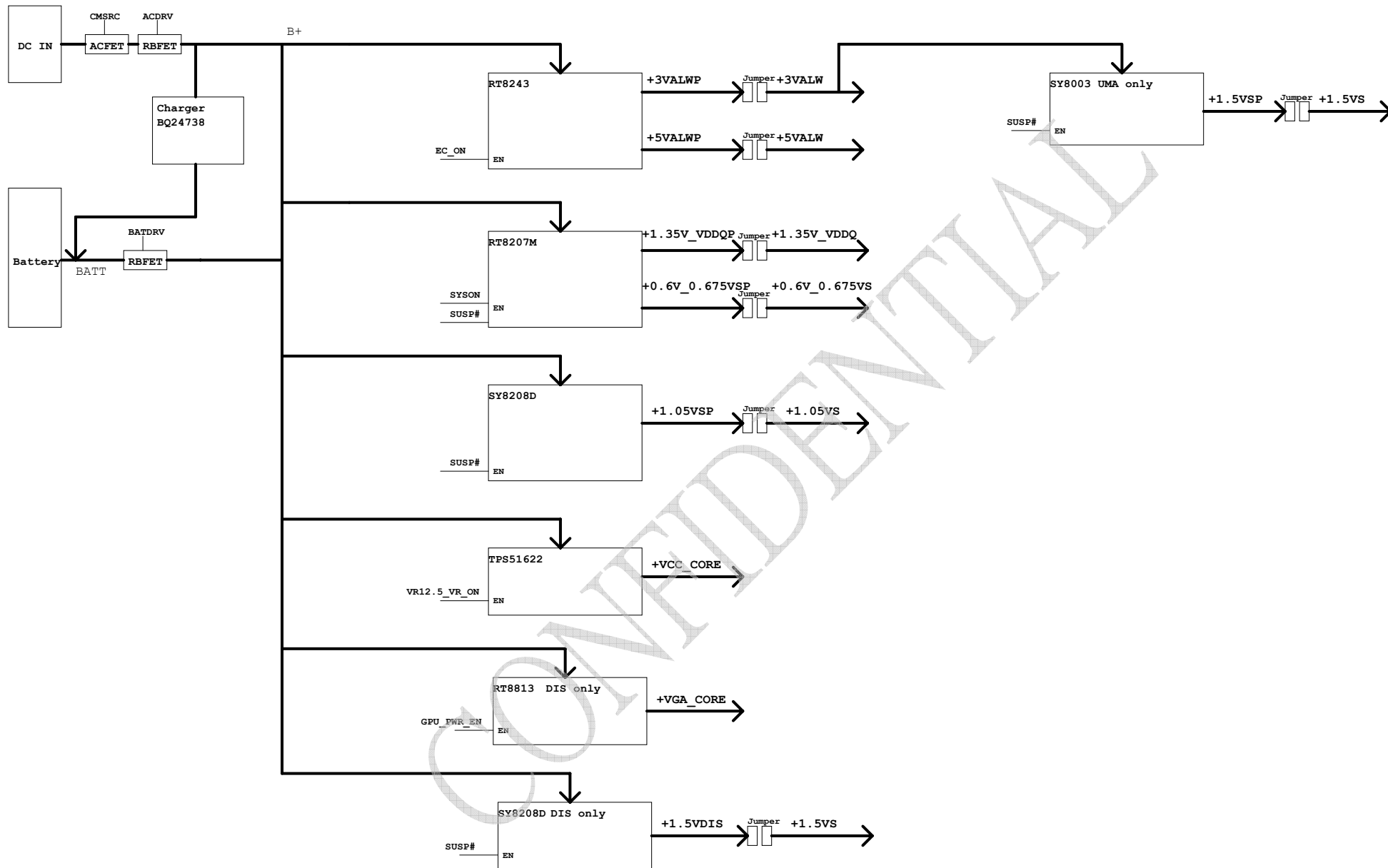
PV# 2013.01.23 Add QB8 abd RL25 to support OBFF
PV# 2013.02.22 Unpop QB4 and RL23 for not support OBFF

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				Document Number		
				LA-A992P		
				Rev 0.1		
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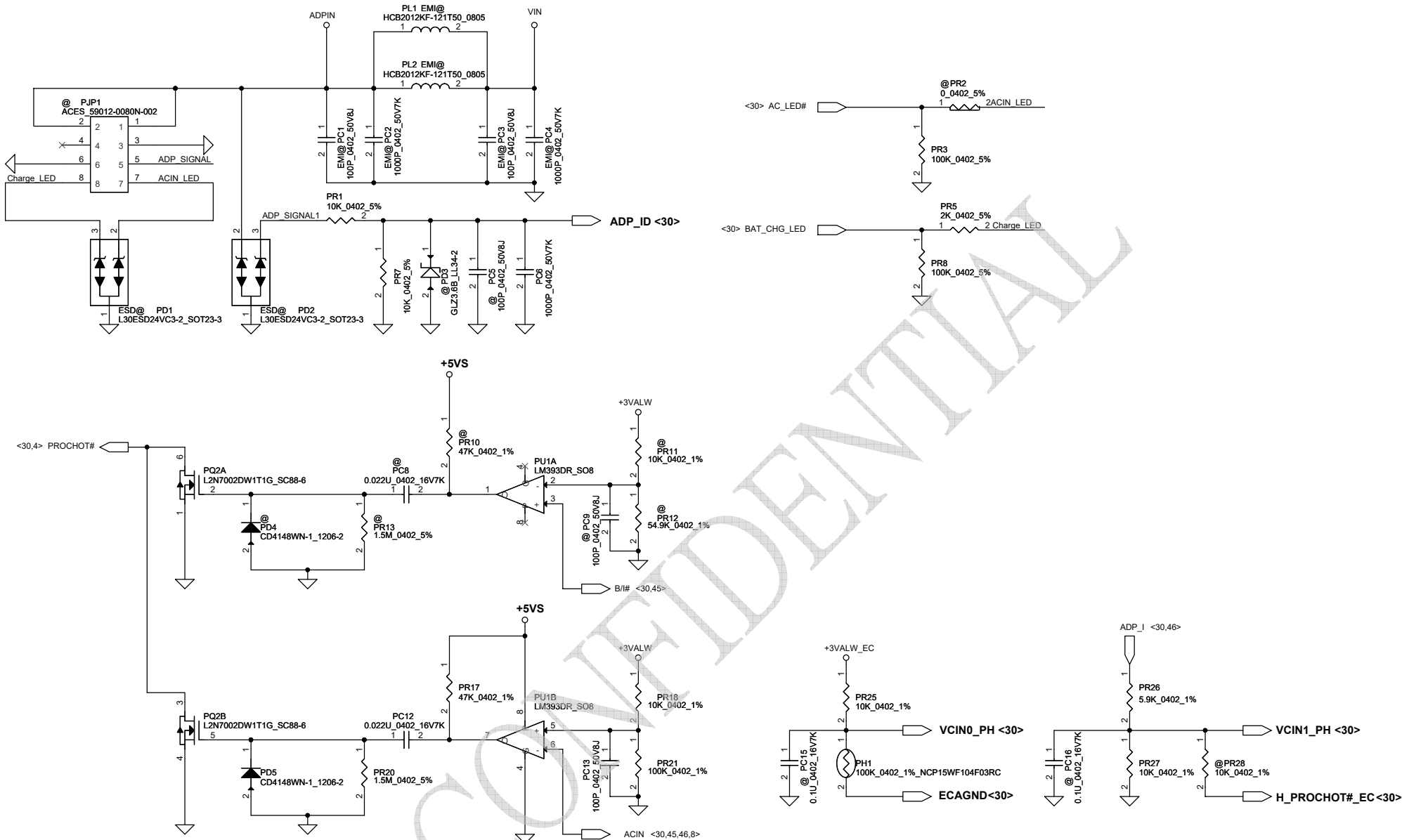
CONFIDENTIAL

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				Sheet 42 of 54	

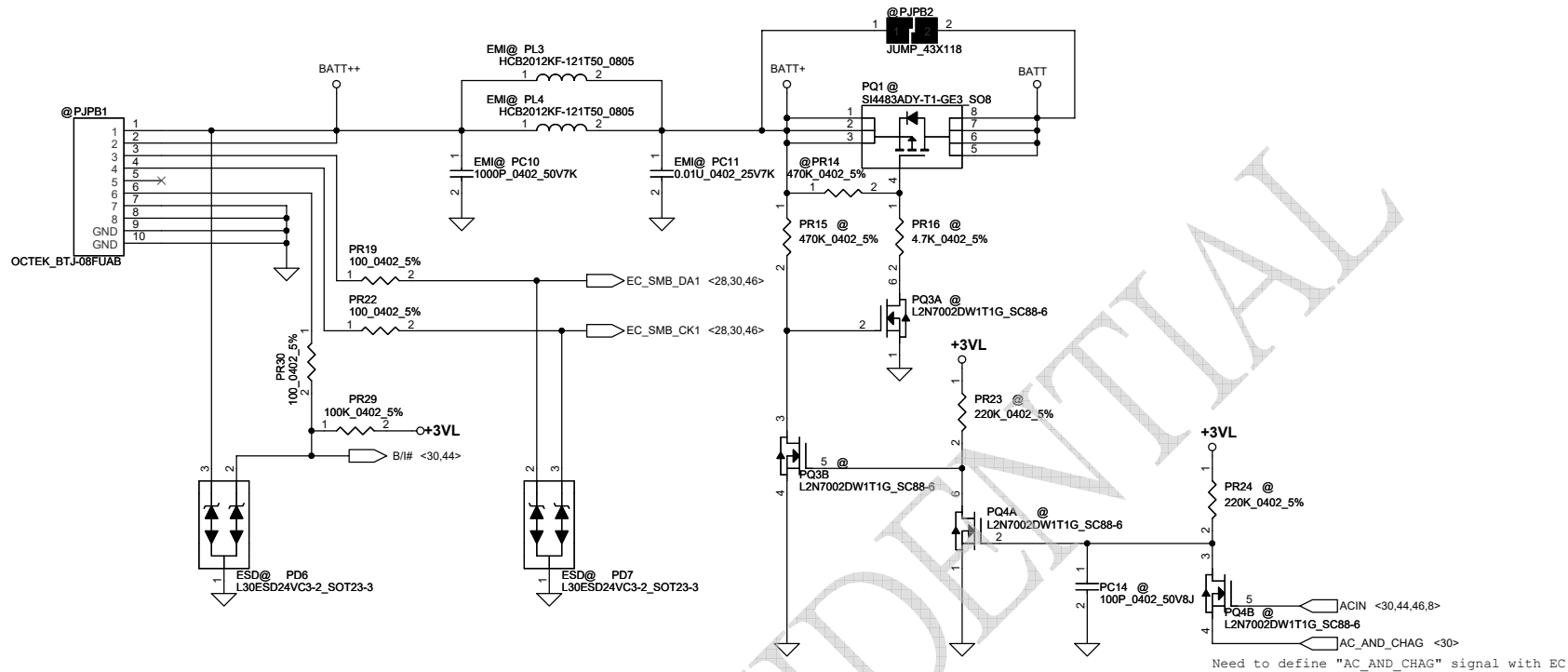


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				Date:	Thursday, March 20, 2014
				Sheet	43 of 55
				Rev	0.4

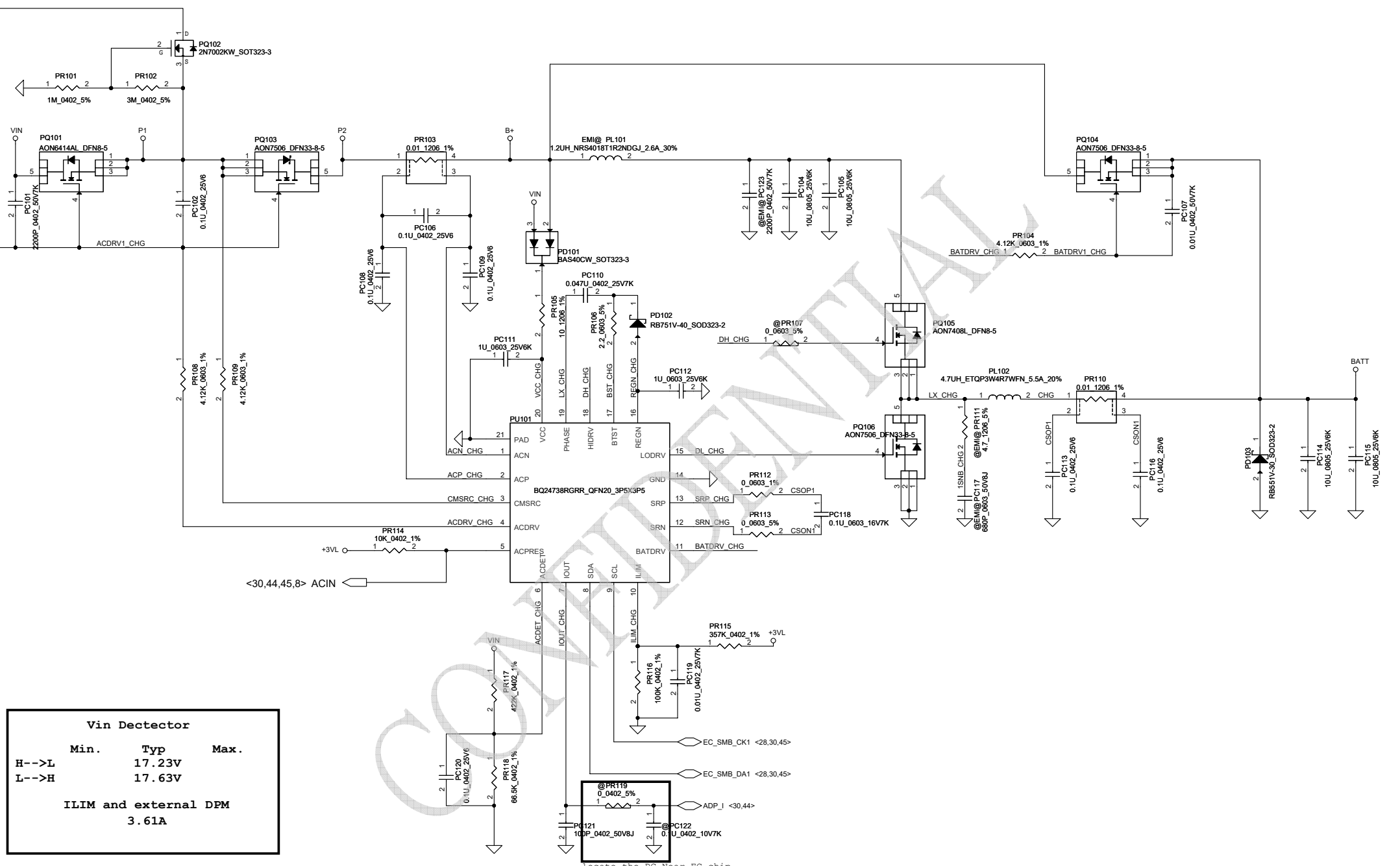
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				Date	Thursday, March 20, 2014
				Sheet	44 of 55
				Rev	0.4

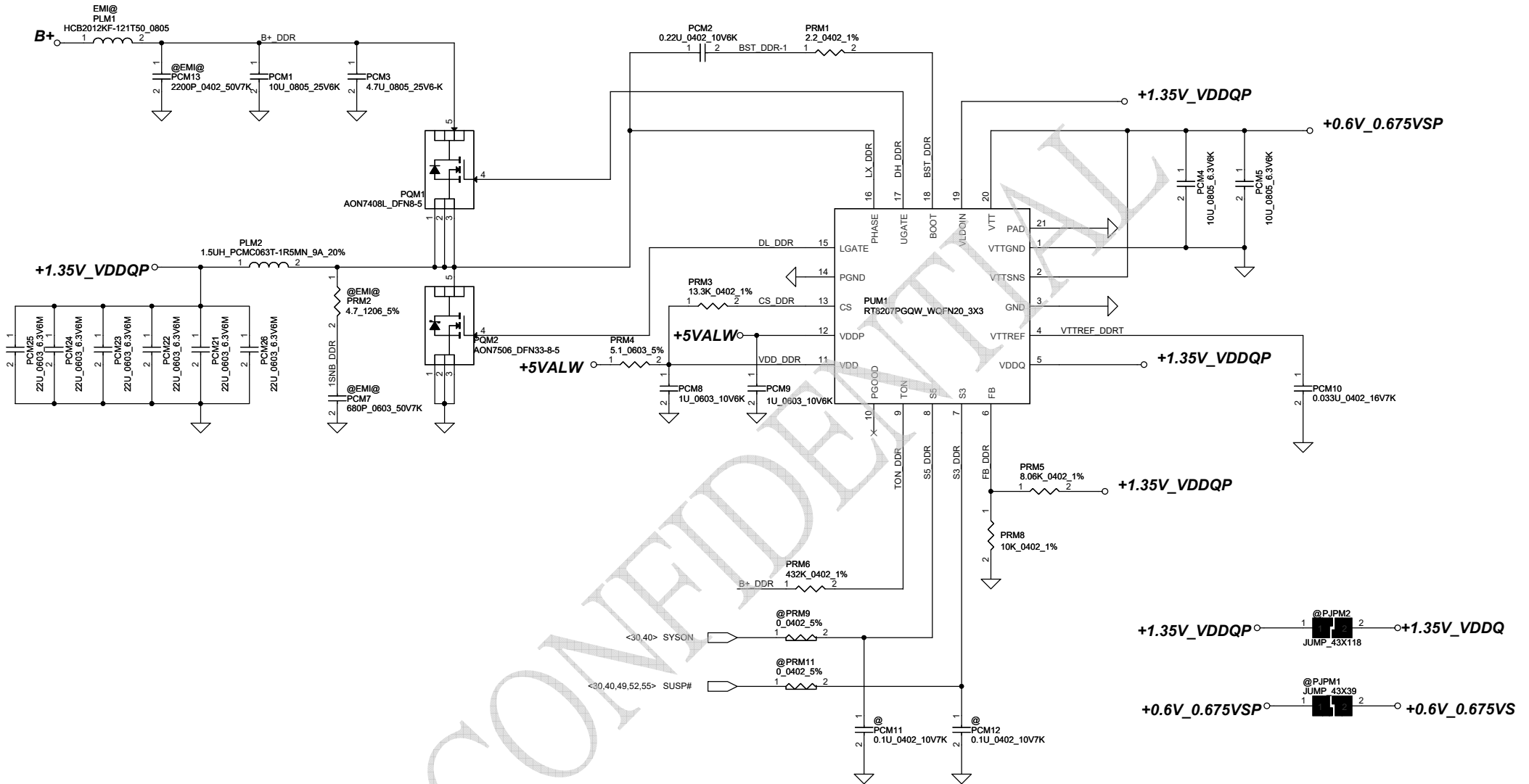


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				Date	Thursday, March 20, 2014
				Sheet	45 of 55
				Rev	0.4



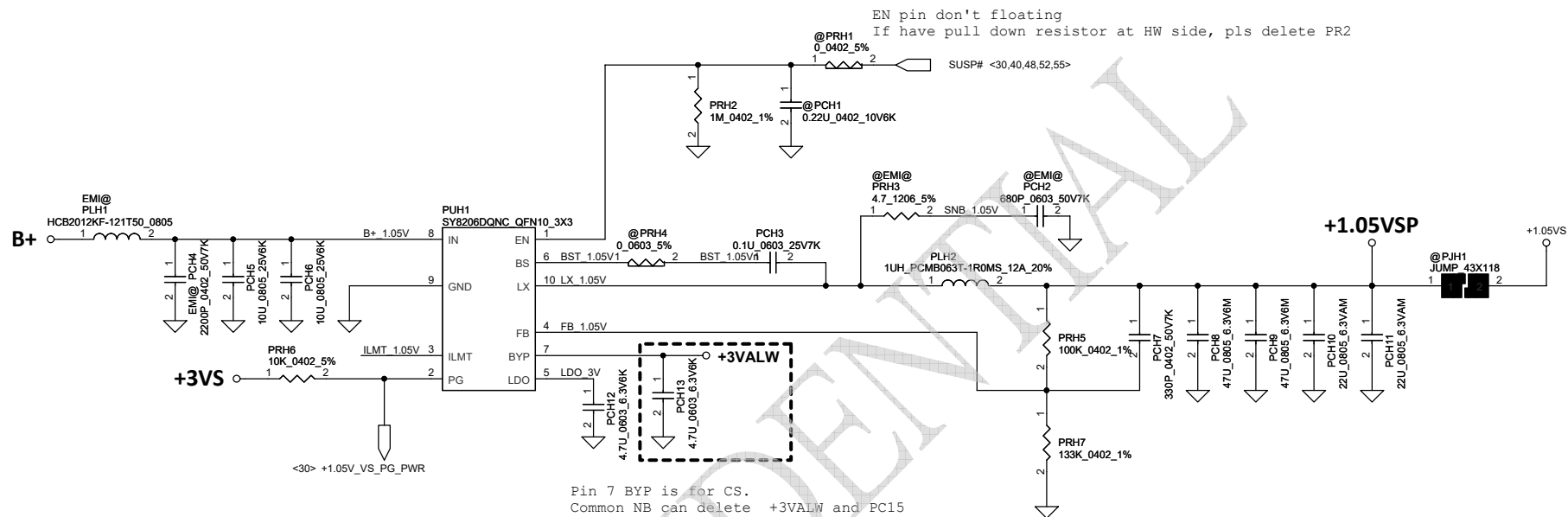
Vin Detector			
	Min.	Typ	Max.
H-->L		17.23V	
L-->H		17.63V	
ILIM and external DPM			
3.61A			

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				Rev	0.4
				Date:	
				Sheet	46 of 55

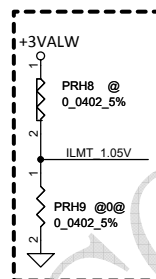


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				Date: Thursday, March 20, 2014	Rev 0.4
				Sheet 48 of 55	

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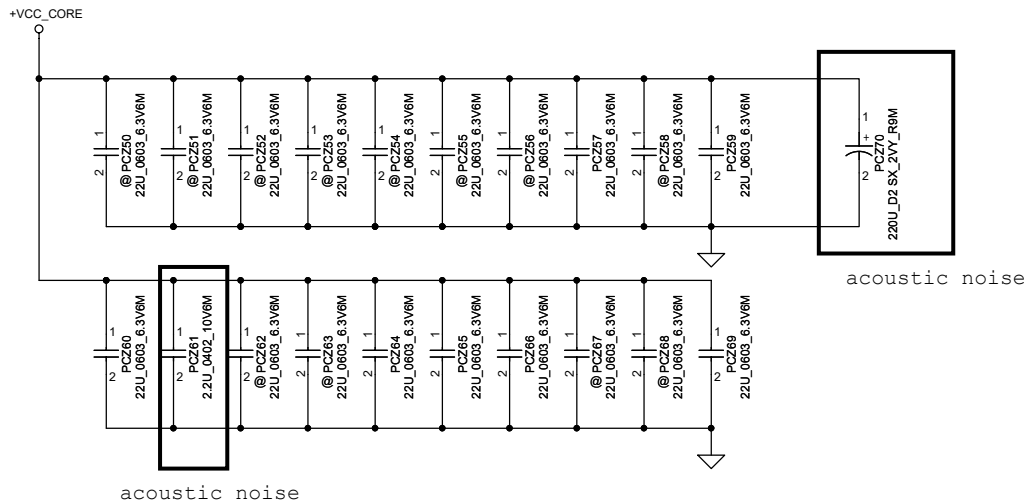
continuous 6A
peak 12A



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

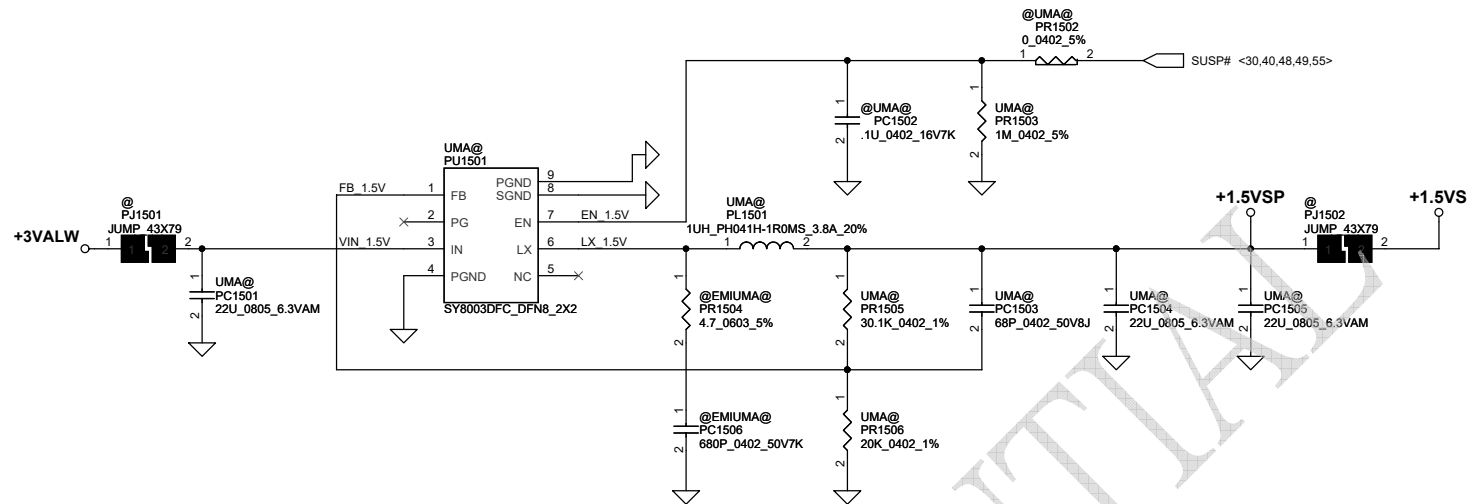
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Issued Date	2013/08/07	Deciphered Date	2016/08/06	Title	1.05V
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				Date	Thursday, March 20, 2014
				Sheet	49 of 55





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				Date	Thursday, March 20, 2014
				Sheet	51 of 55

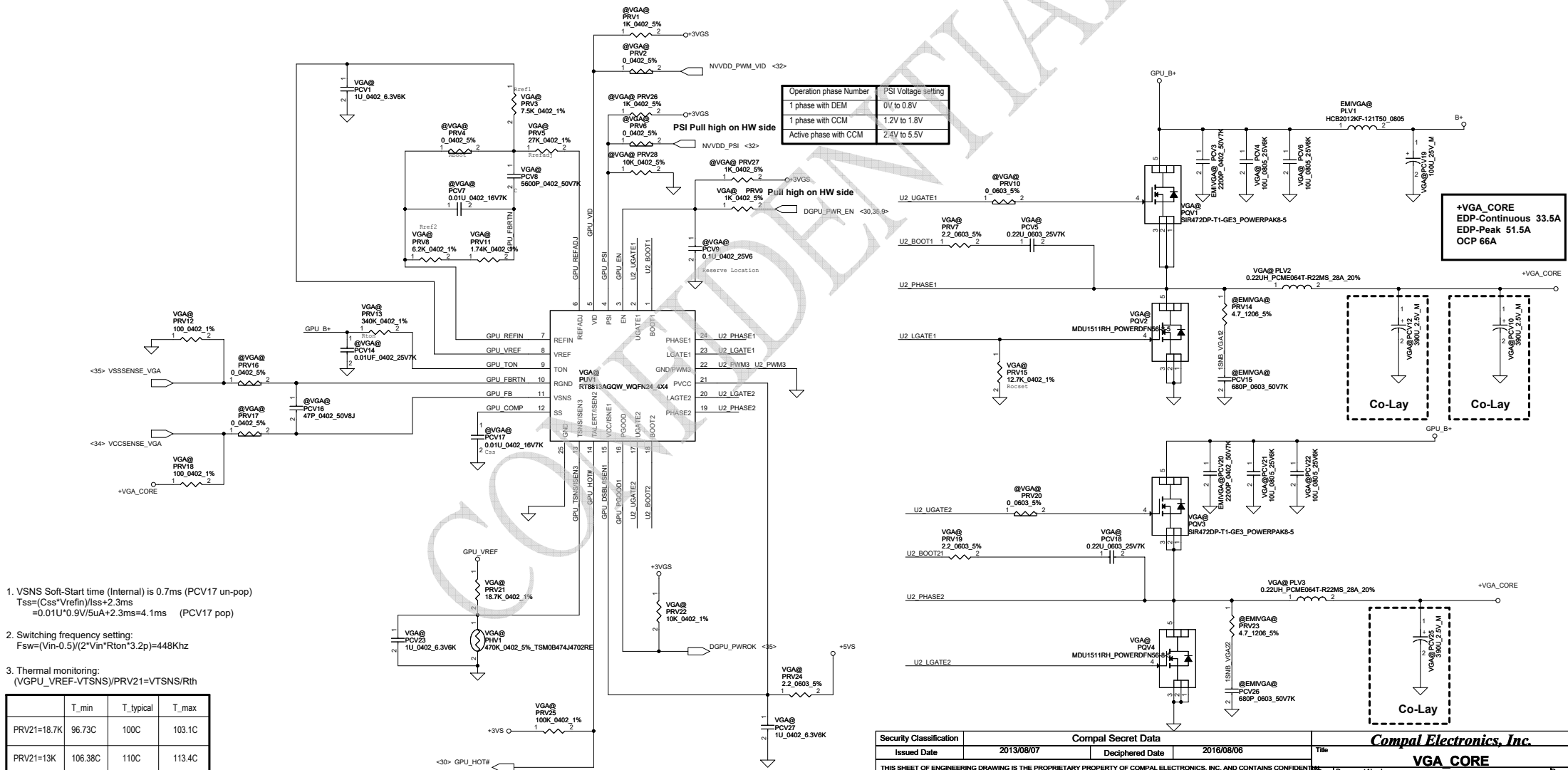
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continuous 3A

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				Date:	Thursday, March 20, 2014
				Sheet	52 of 55
				Rev	0.4

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+VGA_CORE

PLACE UNDER GPU

PLACE NEAR GPU

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